

# ONIX

ASIC Prototyping Platforms



## AVT-ONIX-PCIE-IPASS-8X-G (A) User Guide

Version 0.1

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## 1. Revision History

The following table shows the revision history for this document.

Author / Company	Description	Revision	Date
ONIX D.T Ltd	Initial ONIX release	0.1	01/06/17

*Table 1 – Revision History*

## 2. Reference Documents

Document	Source
iPASS Interconnect Solutions	Molex

*Table 2 – Reference Documents*

### 3. AVT-ONIX-PCIE-IPASS-8X Features

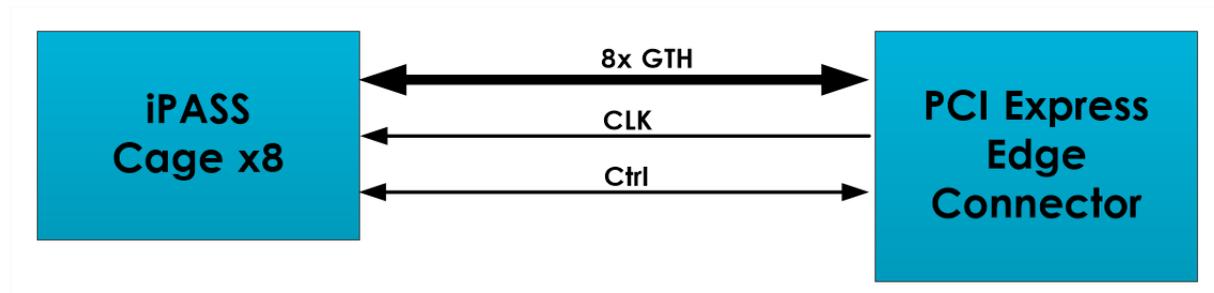
#### 3.1. Overview

This document provides information regarding the AVT-ONIX-PCIE-IPASS-8X adapter. The adapter provides eight lanes up to 8Gbps capable of PCI Express Gen 1,2 and 3. The interconnection is a point to point between PCIe edge connector and iPASS high speed connector by Molex. The board is designed as Low profile cards according to PCI Express specification.

The following chapters will describe the top-down information of PCIE-IPASS Module.

#### 3.2. Block Diagram

The AVT-ONIX-PCIE-IPASS-8X board block diagram is shown in Figure 1.



*Figure 1 - AVT-ONIX-PCIE-IPASS Block Diagram*

### **3.3. Board Features**

- Low profile design according PCI Express specification
- 8x lanes up to 8Gbps for iPASS interface
- 1x PCI Express clock
- WAKE\_B, PERST\_B and PRSNT signals according PCIe standard

### 3.4. Feature Descriptions

The following figure shows the AVT-ONIX-PCIE-IPASS-8X board.



*Figure 2 - AVT-ONIX-PCIE-IPASS-8X – Top Board View*



*Figure 3 - AVT-ONIX-PCIE-IPASS-8X - KIT configuration*

### 3.5. Pin-out

#### 3.5.1. IPASS Interface

The 8x High Speed Lane performs data transfers at the rate of up to 8Gbps (depending Cable type and length and motherboard quality).

##### 3.5.1.1. Clock Signals

The following is the connection pin-out of Clock signals.

PCIE Pin	Signal Name	iPASS Pin	iPASS Pin Name	Note
A13	EDGE_REFCLKP	A14	CREFLK+	CLK to FPGA
A14	EDGE_REFCLKN	A15	CREFLK-	

*Table 3 - Clock Signal Pin-out*

##### 3.5.1.2. Control Signals

The following is the connection pin-out of Control signals.

PCIE Pin	Signal Name	iPASS Pin	iPASS Pin Name	Note
B11	PCIE_WAKE_B	B20	CWAKE#	Output from FPGA
A11	PCIE_PERST_B	B21	CPERST#	Input to FPGA

*Table 4 - Control Signals - Pin-out*

### 3.5.1.3. High Speed Signals

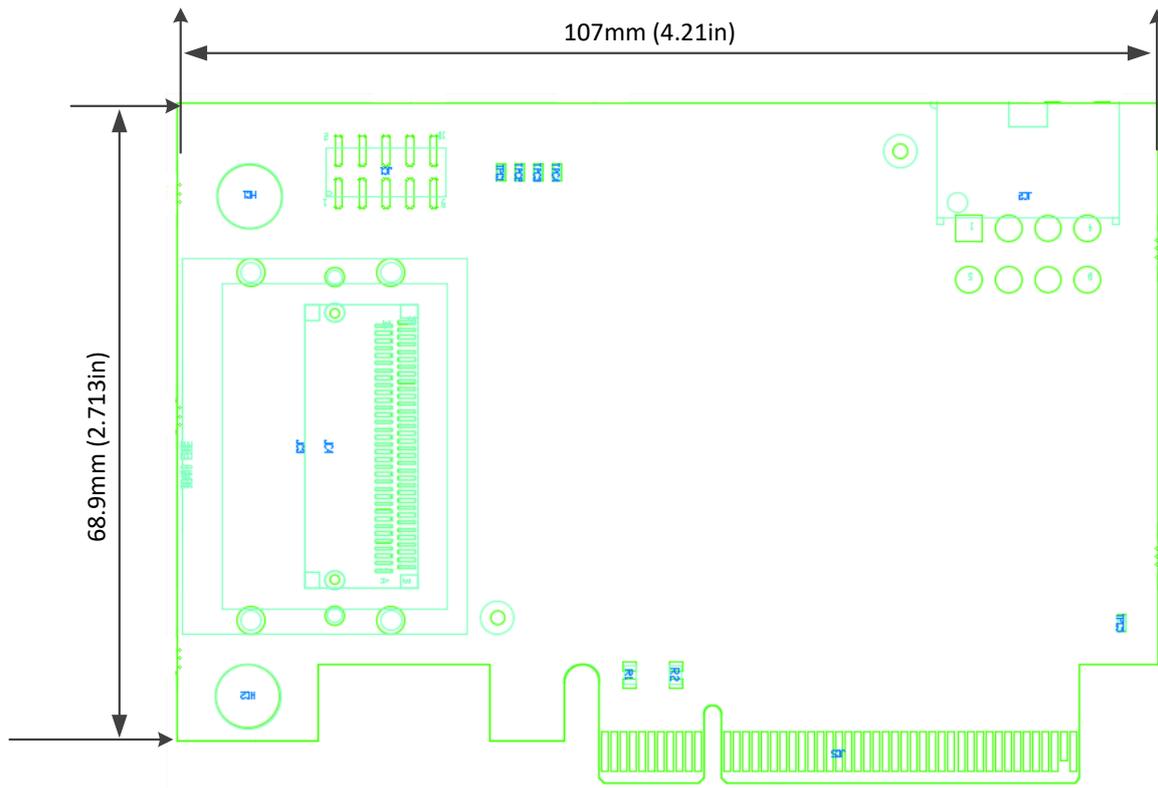
The following is the connection list between the PCIe edge connector and iPASS Connector.

PCIE Pin	Signal Name	iPASS Pin	iPASS Pin Name	Note
A16	PCIE_M2H.0P	B2	PERp0	RX to FPGA
A17	PCIE_M2H.0N	B3	PERn0	
A21	PCIE_M2H.1P	B5	PERp1	RX to FPGA
A22	PCIE_M2H.1N	B6	PERn1	
A25	PCIE_M2H.2P	B8	PERp2	RX to FPGA
A26	PCIE_M2H.2N	B9	PERn2	
A29	PCIE_M2H.3P	B11	PERp3	RX to FPGA
A30	PCIE_M2H.3N	B12	PERn3	
A35	PCIE_M2H.4P	B23	PERp4	RX to FPGA
A36	PCIE_M2H.4N	B24	PERn4	
A39	PCIE_M2H.5P	B26	PERp5	RX to FPGA
A40	PCIE_M2H.5N	B27	PERn5	
A43	PCIE_M2H.6P	B29	PERp6	RX to FPGA
A44	PCIE_M2H.6N	B30	PERn6	
A47	PCIE_M2H.7P	B32	PERp7	RX to FPGA
A48	PCIE_M2H.7N	B33	PERn7	
B14	PCIE_H2M.0P	A2	PETp0	TX from FPGA
B15	PCIE_H2M.0N	A3	PETn0	
B19	PCIE_H2M.1P	A5	PETp1	TX from FPGA
B20	PCIE_H2M.1N	A6	PETn1	
B23	PCIE_H2M.2P	A8	PETp2	TX from FPGA
B24	PCIE_H2M.2N	A9	PETn2	
B27	PCIE_H2M.3P	A11	PETp3	TX from FPGA
B28	PCIE_H2M.3N	A12	PETn3	
B33	PCIE_H2M.4P	A23	PETp4	TX from FPGA
B34	PCIE_H2M.4N	A24	PETn4	
B37	PCIE_H2M.5P	A26	PETp5	TX from FPGA
B38	PCIE_H2M.5N	A27	PETn5	
B41	PCIE_H2M.6P	A29	PETp6	TX from FPGA
B42	PCIE_H2M.6N	A30	PETn6	
B45	PCIE_H2M.7P	A32	PETp7	TX from FPGA
B46	PCIE_H2M.7N	A33	PETn7	

*Table 5 - High Speed Lanes Pin-out*

## 4. Board Specifications

### 4.1. Board Dimensions



*Figure 4 - Module Dimensions*

Notes:

1. All dimensions are in millimeters
2. The dimensional diagram is for reference only

## 5. Order Information

### 5.1. Parts

Part Number	Description	Price
AVT-ONIX-PCIE-IPASS-8X-G	PCI Express to IPASS 8x module	Contact your local distributor

### 5.2. Related Products

Part Number	Description	Price
AVT-ONIX-FMC-IPASS-8X-G	FMC to IPASS 8x Lanes	Contact your local distributor
AVT-ONIX-KIT-IPASS-8X-G	PCI Express over Cable	Contact your local distributor

*\*For more info <http://www.onix.systems>*