# ONIX-FMC-INTF
# User Guide

**Version 0.4**

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## 1. Revision History

The following table shows the revision history for this document.

| Author / Company | Description | Revision | Date |
|---|---|---|---|
| ONIX D.T Ltd | Initial ONIX release | 0.1 | 01/09/16 |
| ONIX D.T Ltd | Updated block diagram design | 0.2 | 08/09/16 |
| ONIX D.T Ltd | Updated Related Products table | 0.3 | 01/11/16 |
| ONIX D.T Ltd | Updated GbE block diagram | 0.4 | 13/02/17 |

*Table 1 – Revision History*

## 2. Reference Documents

| Document | Source |
|---|---|
| FPGA Mezzanine Card (FMC) Standard | VITA |
| Serial ATA Revision 3.0 | Serial ATA |
| Digilent Pmod Interface Specification | Digilent |
| ARM JTAG Interface Specification | Lauterbach |

*Table 2 – Reference Documents*

## 3. AVT-ONIX-FMC-INTR Features

### 3.1.   Overview

This document provides information regarding the AVT-ONIX-FMC-INTR (Interfaces & Peripherals) module. The module is a VITA 57.1 compliant single width FMC HPC, designed for use with ONIX modules and more 57.1 compliant carrier cards.

The following chapters will describe the top-down information of FMC-INTR Module.

### 3.2.   Block Diagram
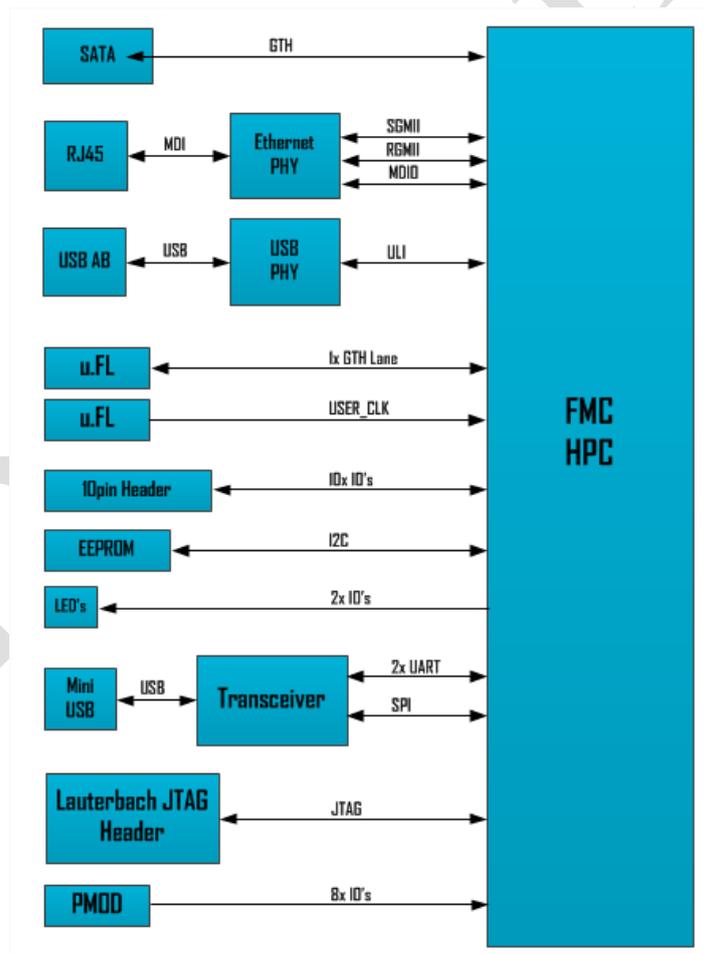
The AVT-ONIX-FMC-INTR board block diagram shown in Figure 1.



*Figure 1 - AVT-ONIX-FMC-INTR Block Diagram*

## 3.3. Board Features

- VITA 57.1 FMC HPC connector

- GbE Interface

- SATA Interface

- USB Interface

- 4x u.FL connector for GTH lane (TX and RX)

- 2x u.FL connector for User clock

- Lauterbach JTAG Header

- PMOD Interface

- 10pin Header for User

- Front Panel LED's

- 2x UART interface (via Transceiver)

- 1x SPI interface (via Transceiver)

- On board clock oscillator for GTH ref clock

## 3.4. Feature Descriptions

The following figure shows the AVT-ONIX-FMC-INTR board. Each numbered feature that is referenced in Figure 2, 3 is described in Table 3.

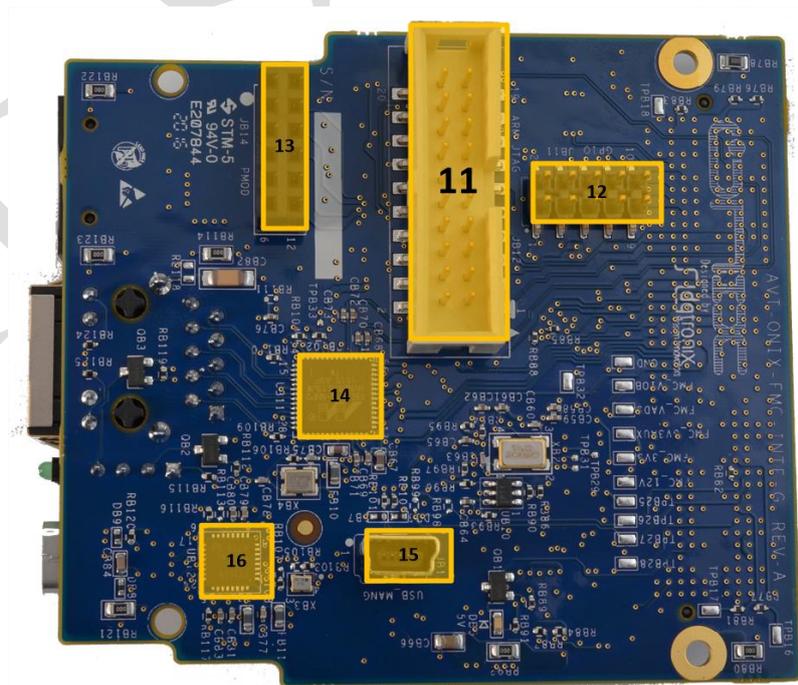*Figure 2 - AVT-ONIX-FMC-INTR – Top Board Components*
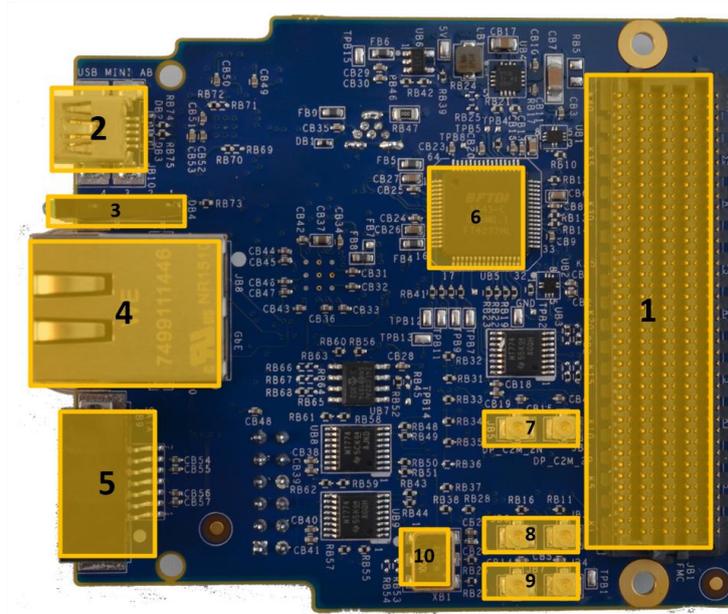


*Figure 3 - AVT-ONIX-FMC-INTR – Bottom Board Components*

| ID | RefDes | Component Description |
|----|--------|----------------------|
| 1 | JB1 | FMC HPC Connector |
| 2 | JB10 | USB Connector |
| 3 | DB4 | Front Panel LED's |
| 4 | JB8 | GbE Connector |
| 5 | JB9 | SATA Connector |
| 6 | UB5 | USB to UART/SPI Transceiver |
| 7 | JB2, JB5 | uFL for GTH Lane (C2M) |
| 8 | JB3, JB6 | uFL for USER input Clock |
| 9 | JB4, JB7 | uFL for GTH Lane (M2C) |
| 10 | XB1 | Oscillator for GTH Ref Clock |
| 11 | JB12 | Lauterbach JTAG Connector |
| 12 | JB11 | 10pin Header for USER IO's |
| 13 | JB14 | PMOD Connector |
| 14 | UB11 | Ethernet PHY |
| 15 | JB13 | USB Connector for UART/SPI I/F |
| 16 | UB12 | USB PHY |

*Table 3 - AVT-ONIX-FMC-INTR Component Descriptions*

### 3.4.1. Gb Ethernet

The board contains Integrated 10/100/1000 Ultra Gigabit Ethernet Transceiver. The PHY P/N is 88E1512-A0-NNP2I000 from Marvell and support on few MAC interface options:

a. RGMII to Copper
b. SGMII to Copper
c. RGMII to Fiber/SGMII
d. RGMII to Copper/Fiber/SGMII with Auto Media Detect

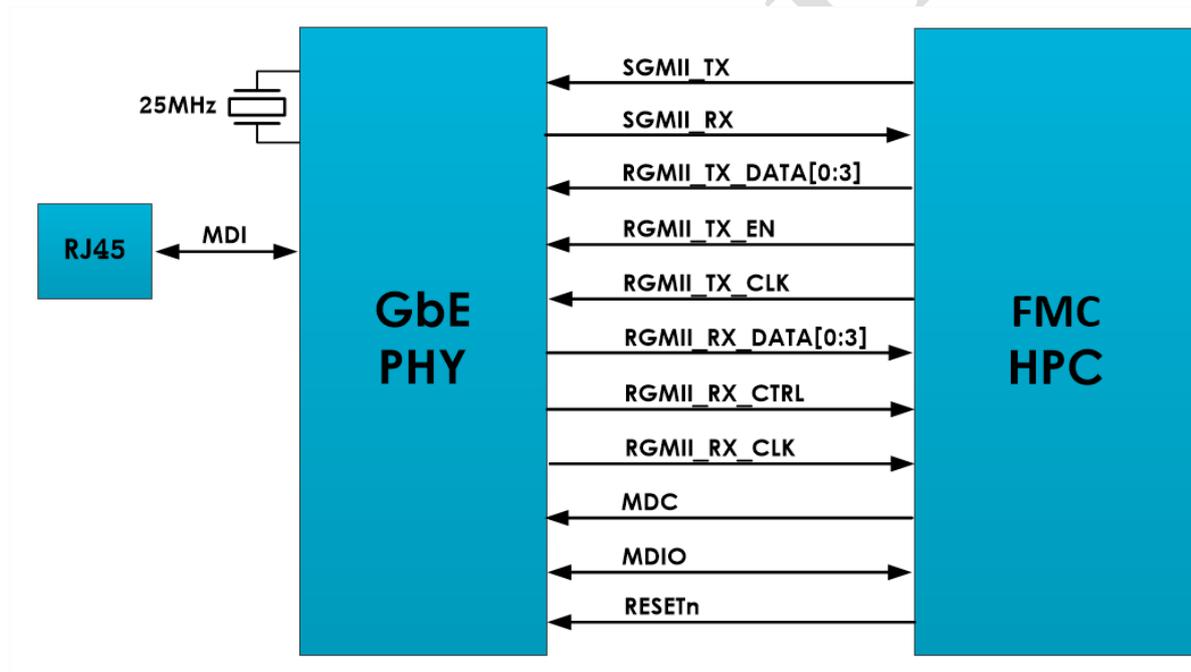The following figure describes the connectivity between the PHY and FMC connector.



*Figure 4 - GbE PHY Connectivity*

The following table is the pin-out between the PHY and FMC connector.

| FMC Pin | Signal Name | Direction | Interface | PHY Pin | Notes |
| --- | --- | --- | --- | --- | --- |
| C2 | SGMII_TXP | Output | SGMII | 1 | From FPGA (GTH) |
| C3 | SGMII_TXN | Output | | 2 | |
| C6 | SGMII_RXP | Input | | 4 | To FPGA (GTH) |
| C7 | SGMII_RXN | Input | | 5 | |
| F7 | RGMII_TXD0 | Input | RGMII | 50 | From FPGA |
| F8 | RGMII_TXD1 | Input | | 51 | From FPGA |
| E6 | RGMII_TXD2 | Input | | 54 | From FPGA |
| E7 | RGMII_TXD3 | Input | | 55 | From FPGA |
| K10 | RGMII_TX_EN | Input | | 56 | From FPGA |
| K11 | RGMII_GTX_CLK | Input | | 53 | From FPGA |
| J6 | RGMII_RXD0 | Output | | 44 | To FPGA |
| K8 | RGMII_RXD1 | Output | | 45 | To FPGA |
| K7 | RGMII_RXD2 | Output | | 47 | To FPGA |
| E3 | RGMII_RXD3 | Output | | 48 | To FPGA |
| E2 | RGMII_RX_DV | Output | | 43 | To FPGA |
| F4 | RGMII_RX_CLK | Output | | 46 | To FPGA |
| J10 | ETH_PHY_MDC | Input | MDIO | 7 | From FPGA |
| J9 | ETH_PHY_MDIO | Bi-Directional | | 8 | From/To FPGA |
| F10 | ETH_RESETn | Input | - | 16 | From FPGA, On board Pull down resistor |

*Table 4 - GbE PHY Pinout*

### 3.4.2.    SATA I/F

The board contains SATA 7Pin signal plug right angle connector. The connector PN is SATA00122073 from Amphenol.

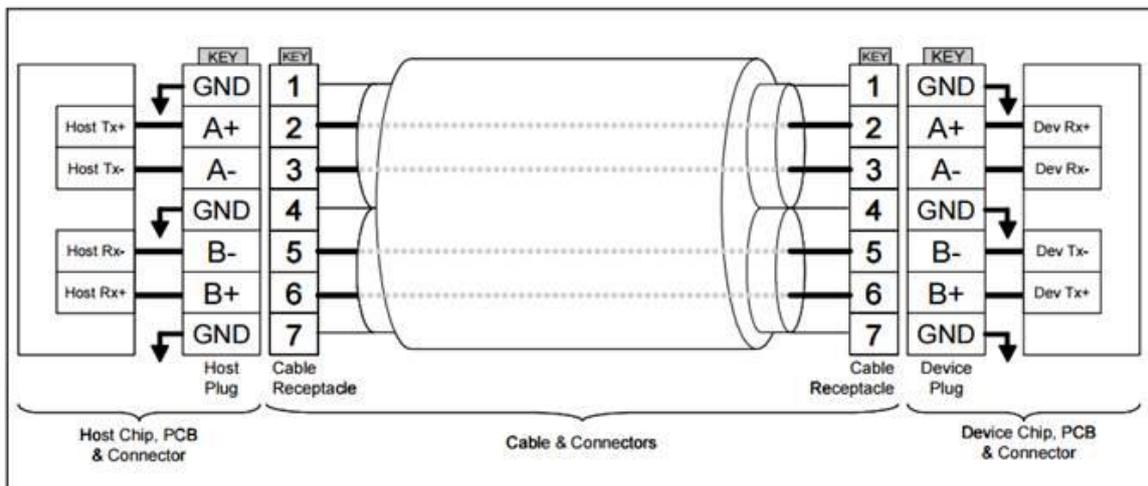The following figure describes the SATA interface between Host and Device.



*Figure 5 - SATA Conectivity*

The following table is the pin-out between SATA and FMC connector.

| FMC Pin | Signal Name | Direction | SATA Pin | Notes |
|---------|-------------|-----------|----------|-------|
| A30 | SATA_TXP | Output | 2 | From FPGA (GTH), On board AC coupling capacitor |
| A31 | SATA_TXN | | 3 | |
| A10 | SATA_RXP | Input | 6 | To FPGA (GTH), On board AC coupling capacitor |
| A11 | SATA_RXN | | 5 | |

*Table 5 - SATA Pin-out*

### 3.4.3.    USB I/F

The board contains USB2.0 PHY Transceiver Chip. The USB PHY P/N is TUSB1210BRHBR from Texas Instruments. The chip designed to interface with a USB Controller through a ULPI interface and Fully Compliant with:

    a.  Universal Serial Bus Specification Rev 2.0

    b.  On-The-Go Supplement to the USB 2.0 Specification Rev 1.3

    c.  UTMI+ Low pin interface (ULPI) Specification Rev1.1

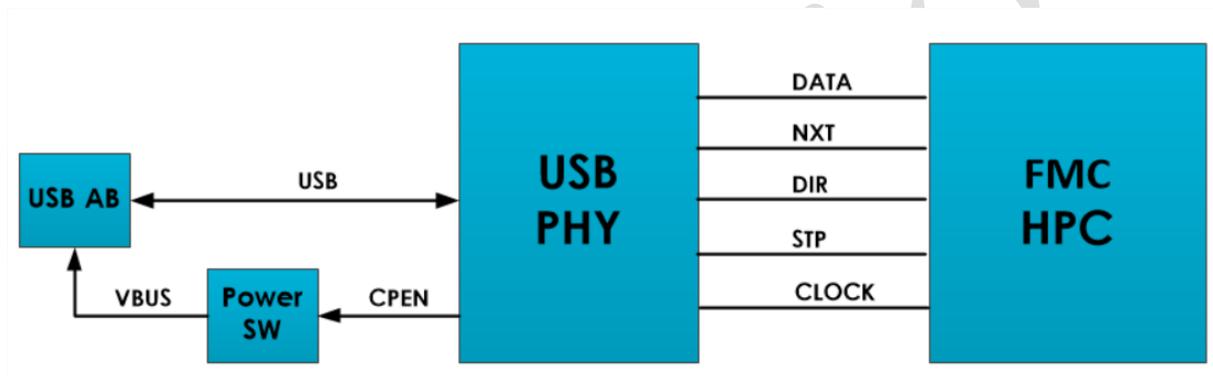The following figure describes the connectivity between the PHY and FMC connector.



*Figure 6 - USB PHY Connectivity*

The following table is the pin-out between the PHY and FMC connector.

| FMC Pin | Signal Name | Direction | I/O Standard | PHY Pin | Notes |
|---------|-------------|-----------|--------------|---------|-------|
| H35 | USB_DATA0 | Bi-Directional | LVCMOS18 | 3 | |
| H34 | USB_DATA1 | Bi-Directional | LVCMOS18 | 4 | |
| G31 | USB_DATA2 | Bi-Directional | LVCMOS18 | 5 | |
| G30 | USB_DATA3 | Bi-Directional | LVCMOS18 | 6 | |
| H32 | USB_DATA4 | Bi-Directional | LVCMOS18 | 7 | |
| H31 | USB_DATA5 | Bi-Directional | LVCMOS18 | 9 | |
| C27 | USB_DATA6 | Bi-Directional | LVCMOS18 | 10 | |
| C26 | USB_DATA7 | Bi-Directional | LVCMOS18 | 13 | |
| G33 | USB_STP | Input | LVCMOS18 | 29 | From FPGA |
| G34 | USB_NXT | Output | LVCMOS18 | 2 | To FPGA |
| H37 | USB_DIR | Output | LVCMOS18 | 31 | To FPGA |
| D20 | USB_CLOCK | Output | LVCMOS18 | 26 | To FPGA |

| D26 | USB_CS | Input | LVCMOS18 | 11 | From FPGA. On board Pull down resistor |
| D27 | USB_RESETB | Input | LVCMOS18 | 27 | From FPGA. On board Pull down resistor |

Notes:

*IO Standard according to ability of FPGA and can be changed depending VADJ voltage of FMC

** There is on board 26MHz CMOS oscillator for PHY reference clock (pin1)

### 3.4.4. PMOD I/F

The PMOD interface is used to connect low frequency, low I/O pin count peripheral module to the host controller boards. There are six-pin and twelve-pin versions of the interface defined.. The twelve-pin version provides eight I/O signals pins, two power pins and two ground pins. The signals of the twelve-pin version are arranged so that it provides two of the six-pin interfaces stacked.
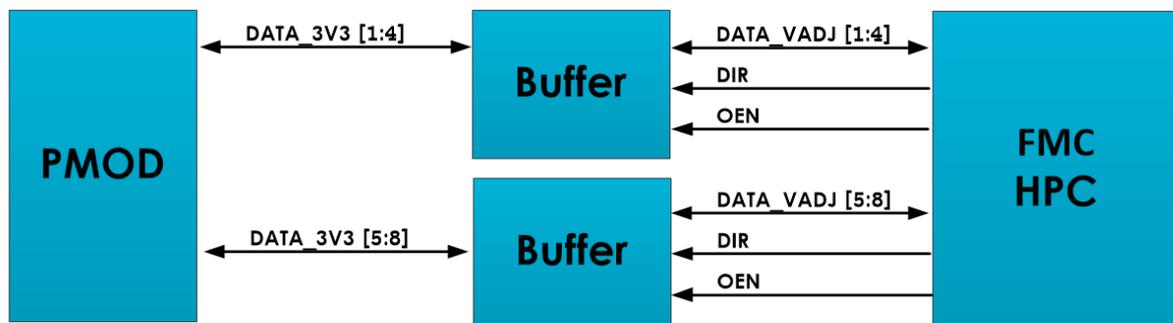


*Figure 7 - PMOD Connectivity*

The PMOD signals translator to/from 3V3 through dedicated buffer (SN74AVC4T774PWR from TI). The buffer is 4-Bit dual supply bus with configurable voltage translation and 3-state outputs.

The following is functional table for control inputs that select the direction of the IO and Enable/Disable the outputs.

| CONTROL INPUTS | | OUTPUT CIRCUITS | | OPERATION |
|---|---|---|---|---|
| $\overline{OE}$ | DIR | A PORT | B PORT | |
| L | L | Enabled | Hi-Z | B data to A data |
| L | H | Hi-Z | Enabled | A data to B data |
| H | X | Hi-Z | Hi-Z | Isolation |

*Table 6 - Buffer Functional Table*

The following list is the twelve-pin-out of the PMOD connector.

| FPGA Pin | Signal | Direction | IO Standard | PMOD Pin Number | Notes |
|----------|--------|-----------|-------------|-----------------|-------|
| F16 | GPIO_ADJ_01 | In/Out | LVCMOS_VADJ | 1 | - |
| F17 | GPIO_ADJ_02 | In/Out | LVCMOS_VADJ | 2 | - |
| E15 | GPIO_ADJ_03 | In/Out | LVCMOS_VADJ | 3 | - |
| E16 | GPIO_ADJ_04 | In/Out | LVCMOS_VADJ | 4 | - |
| - | GND | - | | 5 | - |
| - | FMC_3V3 | - | | 6 | - |
| F20 | GPIO_ADJ_05 | In/Out | LVCMOS_VADJ | 7 | - |
| E18 | GPIO_ADJ_06 | In/Out | LVCMOS_VADJ | 8 | - |
| E19 | GPIO_ADJ_07 | In/Out | LVCMOS_VADJ | 9 | - |
| K19 | GPIO_ADJ_08 | In/Out | LVCMOS_VADJ | 10 | - |
| - | GND | - | | 11 | - |
| - | FMC_3V3 | - | | 12 | - |
| F19 | GPIO_Q1_OEN | Output | LVCMOS_VADJ | - | On board PD resistor |
| K16 | GPIO_01_DIR1 | Output | LVCMOS_VADJ | - | On board PD resistor |
| K17 | GPIO_02_DIR2 | Output | LVCMOS_VADJ | - | On board PD resistor |
| J18 | GPIO_03_DIR3 | Output | LVCMOS_VADJ | - | On board PD resistor |
| J19 | GPIO_04_DIR4 | Output | LVCMOS_VADJ | - | On board PD resistor |
| K23 | GPIO_Q2_OEN | Output | LVCMOS_VADJ | - | On board PD resistor |
| K20 | GPIO_05_DIR1 | Output | LVCMOS_VADJ | - | On board PD resistor |
| J21 | GPIO_06_DIR2 | Output | LVCMOS_VADJ | - | On board PD resistor |
| J22 | GPIO_07_DIR3 | Output | LVCMOS_VADJ | - | On board PD resistor |
| K22 | GPIO_08_DIR4 | Output | LVCMOS_VADJ | - | On board PD resistor |

*Table 7 - PMOD Pin-out*

### 3.4.5.    USB to UART Bridge

The AVT-ONIX-FMC-INTR board contains a FTDI FT4232HL USB to UART bridge device (UA5) which allows a connection between host computer and FPGA with a USB port. The USB cable (standard-A plug to host computer and mini-B plug to JA13 connector) is supplied in the Kit.

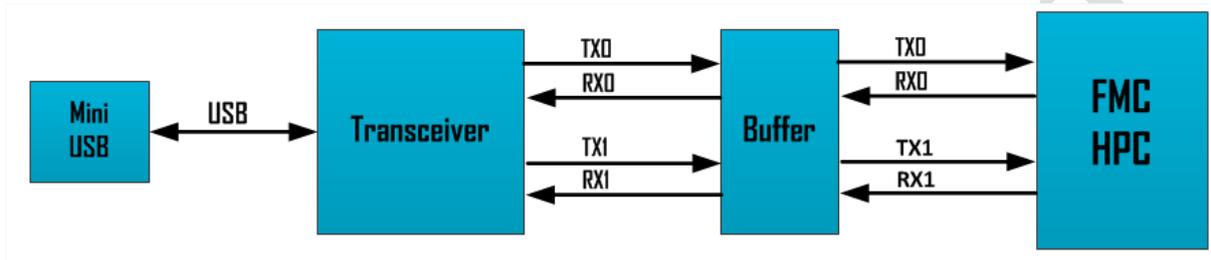The following figure describes the connectivity of UART interface.



*Figure 8 - USB to UART Bridge connectivity*

The following is the connection between FPGA and UART.

| FMC Pin | Signal Name | Direction | I/O Standard | Note |
|---------|-------------|-----------|--------------|------|
| D11 | UART0_TXD | Output | LVCMOS | To FPGA |
| H10 | UART0_RXD | Input | LVCMOS | From FPGA |
| D12 | UART0_TXD | Output | LVCMOS | To FPGA |
| H11 | UART0_RXD | Input | LVCMOS | From FPGA |

| FTDI Device UA5 | | |
|-----|----------|-----------|
| Pin | Function | Direction |
| 39 | RX | Input |
| 38 | TX | Output |
| 52 | RX | Input |
| 48 | TX | Output |

*Table 8 - USB to UART Pin-out*

### 3.4.6. USB to SPI Bridge

The AVT-ONIX-FMC-INTR board contains a FTDI FT4232HL USB to SPI bridge device (UA5) which allows a connection between host computer and FPGA with a USB port. The USB cable (standard-A plug to host computer and mini-B plug to JA13 connector) is supplied in the Kit.

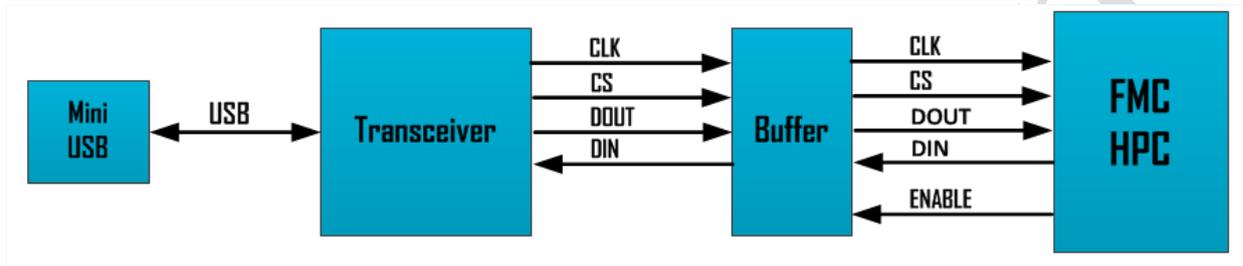The following figure describes the connectivity of SPI interface.



*Figure 9 - USB to SPI Bridge connectivity*

The following is the connection between FPGA and SPI.

| FMC Pin | Direction | IO Standard | Net Name | Note |
|---------|-----------|-------------|----------|------|
| G6 | Output | LVCMOS | SPIB_CLK_VADJ | SPI Clock - input to FPGA |
| H7 | Output | LVCMOS | SPIB_DO_VADJ | SPI Dout - inout to FPGA |
| G9 | Output | LVCMOS | SPIB_CS_VADJ | SPI Chip Select - input to FPGA |
| H8 | Input | LVCMOS | SPIB_DI_VADJ | SPI Din - Output from FPGA |
| G10 | Input | LVCMOS | SPIB_OEN | Enable = 1 \ Disable = 0 for SPI Buffer, Default = 0 |

| FTDI Device UA5 | | |
|-----|----------|-----------|
| **Pin** | **Function** | **Direction** |
| 26 | CLK | Output |
| 27 | DO | Output |
| 28 | DI | Input |
| 29 | CS | Output |

*Table 9 - USB to SPI Pin-out*

### 3.4.7. Lauterbach I/F

The board includes Lauterbach I/F JTAG connector. The Lauterbach debugger communicates with the processor via JTAG interface. The connector is a male standard 20-pin double row connector (two rows of ten pins), pitch 0.1in.

The following is the mechanical connector is specified by ARM (ARM-20)

| Signal | Pin | Pin | Signal |
|--------|-----|-----|--------|
| VTREF | 1 | 2 | VSUPPLY(not used) |
| TRST- | 3 | 4 | GND |
| TDI | 5 | 6 | GND |
| TMS | 7 | 8 | GND |
| TCK | 9 | 10 | GND |
| RTCK | 11 | 12 | GND |
| TDO | 13 | 14 | GND |
| SRST- | 15 | 16 | GND |
| DBGRQ | 17 | 18 | GND |
| DBGACK | 19 | 20 | GND |

The following is the pin-out between Lauterbach and FMC connector.

| FMC Pin | Signal Name | Direction | Lauterbach Pin | Notes |
|---------|-------------|-----------|----------------|-------|
| C10 | ARM_TRSTn | Output | 3 | To FPGA |
| C11 | ARM_TDI | Output | 5 | To FPGA |
| H13 | ARM_TMS | Output | 7 | To FPGA |
| D8 | ARM_TCK | Output | 9 | To FPGA |
| G12 | ARM_RTCK | Input | 11 | From FPGA |
| G13 | ARM_TDO | Input | 13 | From FPGA |
| D14 | ARM_SRSTn | Bi-Directional | 15 | - |
| D15 | ARM_DBGRQ | Output | 17 | To FPGA |
| C14 | ARM_DBGACK | Input | 19 | From FPGA |

*Table 10 - Lauterbach Pin-out*

*For more info please see in ARM JTAG Interface Specification

### 3.4.8. Panel LED's

The AVT-ONIX-FMC-INTR board contains two panel LED's. The function of each LED's describes on the below table.

| FMC Pin | Function | IO Standard | Color | Controlled by |
|---------|----------|-------------|-------|---------------|
| D9 | Panel LED Top | LVCMOS | Green | FPGA |
| G7 | Panel LED Bottom | LVCMOS | Green | FPGA |

*Table 11 - Panel LED's*

*This Document contains confidential and proprietary information of ONIX D.T Ltd.*

### 3.4.9. U.FL Connectors

The board contains six uFL connectors for the following:

1. GTH Lane TX and RX
2. USER input clock

| FMC Pin | IO Standard | RefDes | Signal Name |
|---|---|---|---|
| H4 | LVDS | JB3 | UFL_FPGA_CLKIN_P |
| H5 | | JB6 | UFL_FPGA_CLKIN_N |
| A26 | - | JB2 | UFL_DP_C2M.2P |
| A27 | | JB5 | UFL_DP_C2M.NP |
| A6 | - | JB4 | UFL_DP_M2C.2P |
| A7 | | JB7 | UFL_DP_M2C.2N |

*Table 12 - User uFL connectors Pin-out*

### 3.4.10. GPIO's Header

The following is the connection between the USER Header and FMC connector.

| FMC Pin | RefDes | Signal Name |
|---------|--------|-------------|
| H16 | JB11.1 | GPIO_1V8_01 |
| H17 | JB11.2 | GPIO_1V8_02 |
| G15 | JB11.3 | GPIO_1V8_03 |
| G16 | JB11.4 | GPIO_1V8_04 |
| D17 | JB11.5 | GPIO_1V8_05 |
| D18 | JB11.6 | GPIO_1V8_06 |
| C18 | JB11.7 | GPIO_1V8_07 |
| C19 | JB11.8 | GPIO_1V8_08 |
| H19 | JB11.9 | GPIO_1V8_09 |
| H20 | JB11.10 | GPIO_1V8_10 |

*Figure 10 - GPIO Header pin-out*

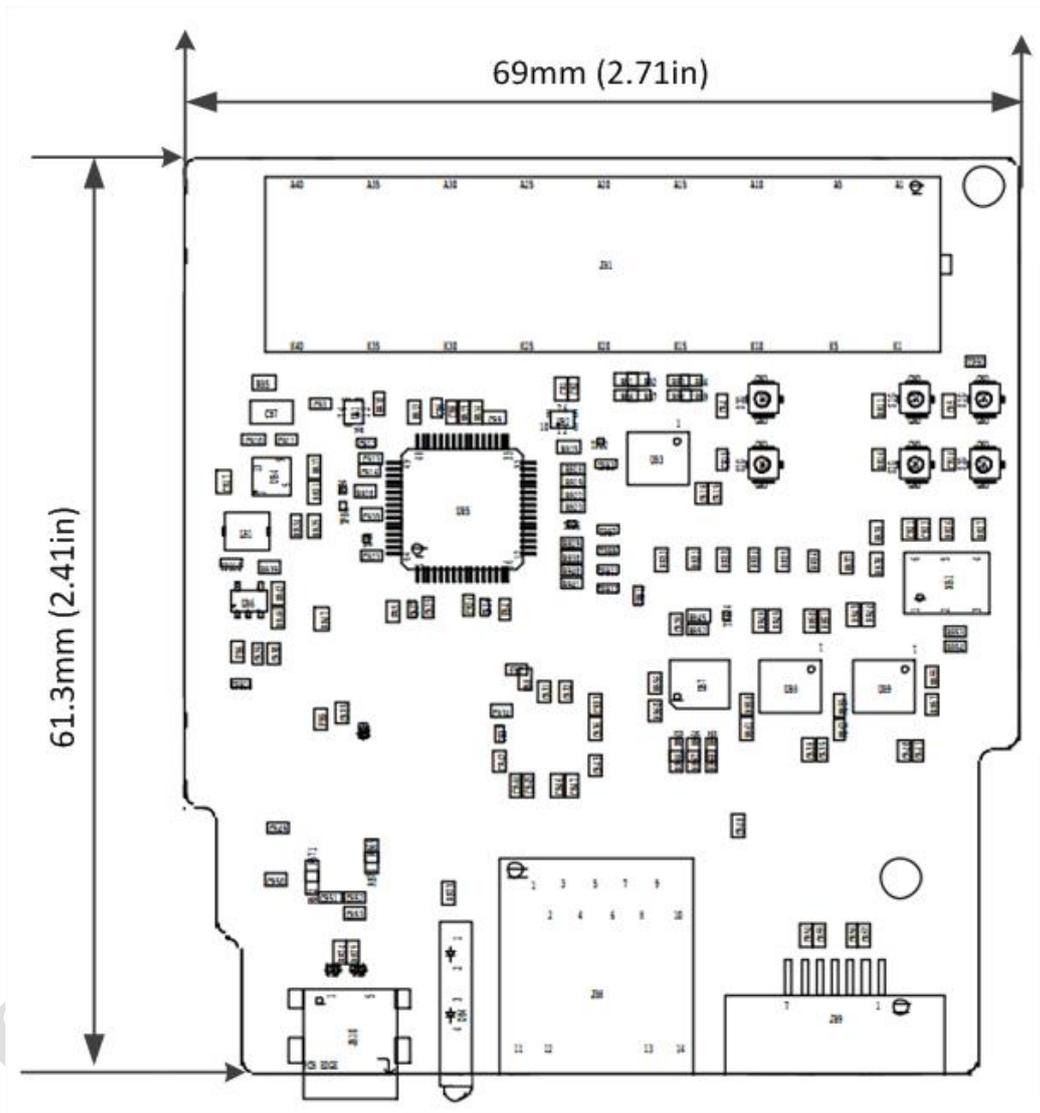# 4. Board Specifications

## 4.1. Board Dimensions



*Figure 11 - Module Dimensions*

Notes:

1. All dimensions are in millimeters

2. The dimensional diagram is for reference only

# 5. Order Information

## 5.1. Parts

| Part Number | Description | Price |
|---|---|---|
| AVT-ONIX-FMC-INTR-G | FMC to Interfaces & Peripherals | Contact your local distributor |

## 5.2. Related Products

| Part Number | Description | Price |
|---|---|---|
| AVT-ONIX-VU440-1 | ONIX Module XCVU440 -1 Device | Contact your local distributor |
| AVT-ONIX-VU440-2 | ONIX Module XCVU440 -2   Device | |
| AVT-ONIX-VU440-3 | ONIX Module XCVU440 -3   Device | |
| AVT-ONIX-FMC-IPASS-8X-G | ONIX FMC to iPASS x8 Adapter | |
| AVT-ONIX-PCIE-IPASS-8X-G | ONIX PCIE to IPASS x8 Adapter | |
| AVT-ONIX-KIT-IPASS-8X-G | PCI Express Over Cable | |

*For more info [http://www.onix.systems](http://www.onix.systems)*