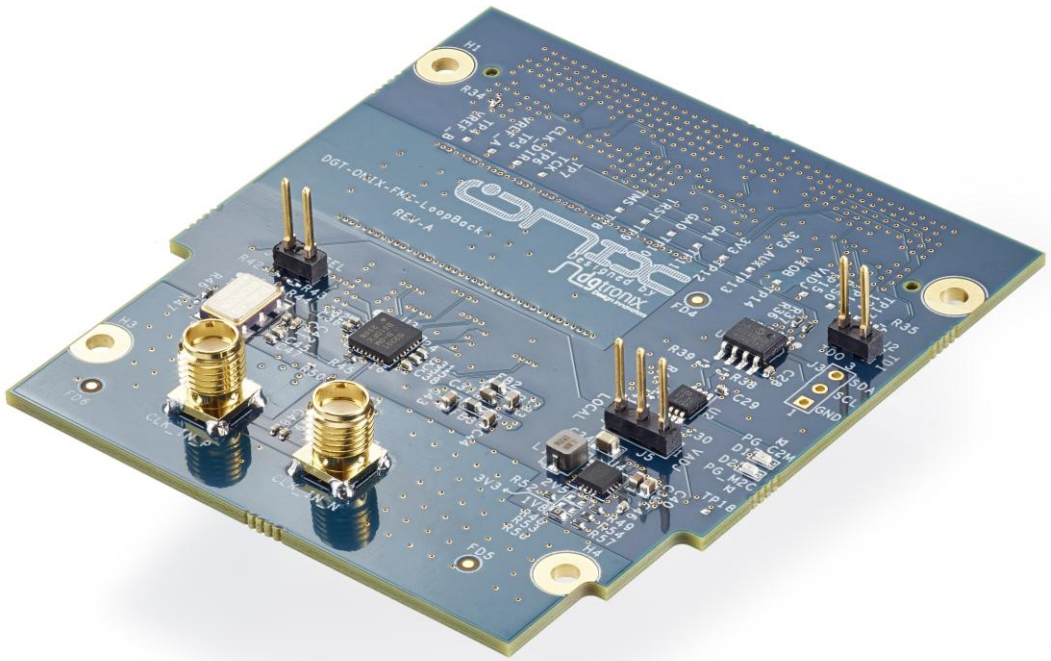
ASIC Prototyping Platforms



ONIX-FMC-LOOPBACK
User Guide

Version 0.3

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Tables

1. Revision History

The following table shows the revision history for this document.

Author / Company	Description	Revision	Date
ONIX D.T Ltd	Initial ONIX release	0.1	25/10/2020
ONIX D.T Ltd	Addition of board pictures	0.2	05/11/2023
ONIX D.T Ltd	Add pictures on chapter 3.4	0.3	05/12/2023

Table 1 – Revision History

2. Reference Documents

Document	Source
FPGA Mezzanine Card (FMC) Standard VITA57.1 Specification	VITA

Table 2 – Reference Documents

3. DGT-ONIX-FMC-LOOPBACK Features

3.1. Overview

This document describes the DGT-ONIX-FMC-LOOPBACK board.

3.2. Block Diagram

Figure 1 shows the block diagram of the DGT-ONIX-FMC-LOOPBACK board.

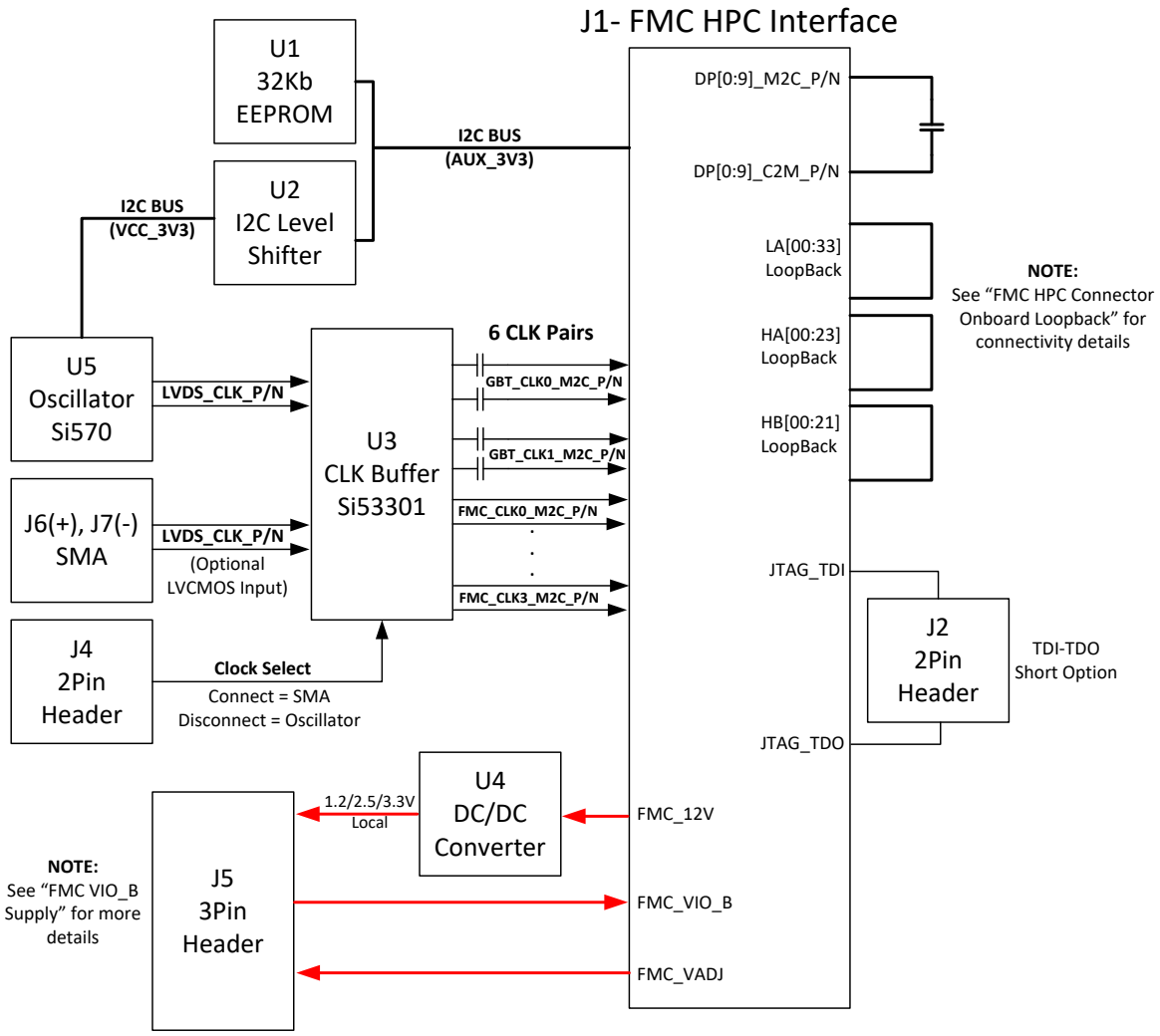


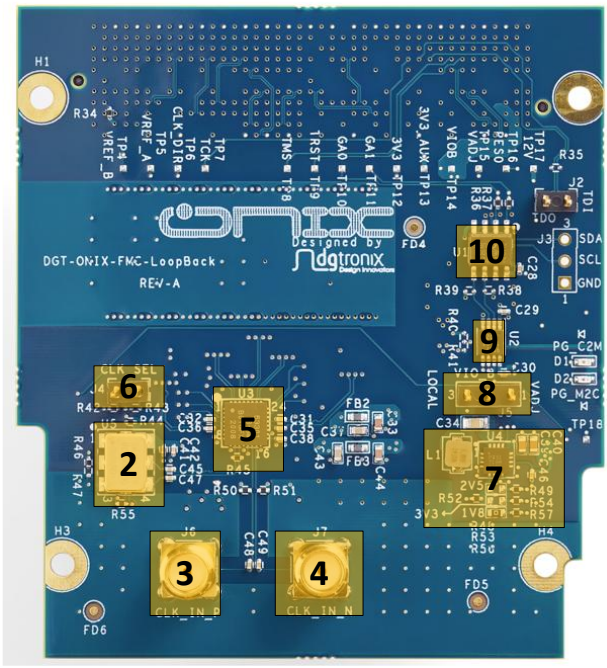
Figure 1 - DGT-ONIX-FMC-LOOPBACK Block Diagram

3.3. Board Features

- VITA 57.1 HPC FMC connector.
- Hard-wired loopback for LA[00:33], HA[00:23], HB[00:21] and DP[0:9] signals.
- Onboard DC/DC converter for VIO_B_M2C.
- 2 x SMA connectors for reference clock input.
- 32Kb I2C EEPROM.
- 6 reference clocks for GBTCLK[1:0]_M2C_P/N and CLK[3:0]_M2C_P/N.

3.4. Feature Descriptions

The following figure shows the DGT-ONIX-FMC-LOOPBACK board. Each numbered feature that is referenced in Figure 2 and Figure 3 is described in Table 3.



ID	RefDes	Component Description
1	J1	VITA 57.1 FMC HPC Connector
2	U5	Si570 serial I2C bus programmable XO (100MHz Default)
3	J6	Positive input - differential reference CLK
4	J7	Negative input - differential reference CLK
5	U3	Si53301 2:6 low-jitter Fanout Clock Buffer
6	J4	Reference Clock Source Header
7	U4	On-Board DC/DC Converter for VIO_B
8	J5	VIO_B Source Header
9	U2	I2C Level Translator
10	U1	32Kbit I2C EEPROM
11	J2	JTAG Loop Header

Table 3.

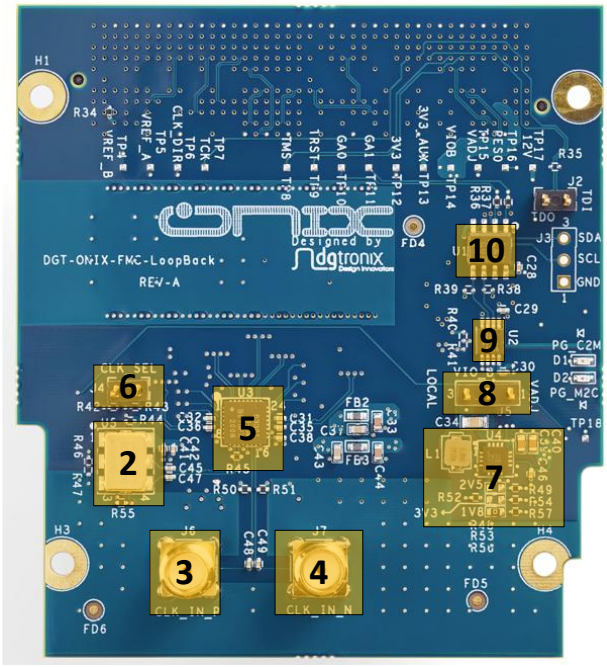


Figure 2: DGT-ONIX-FMC-LOOPBACK – Top Side Components

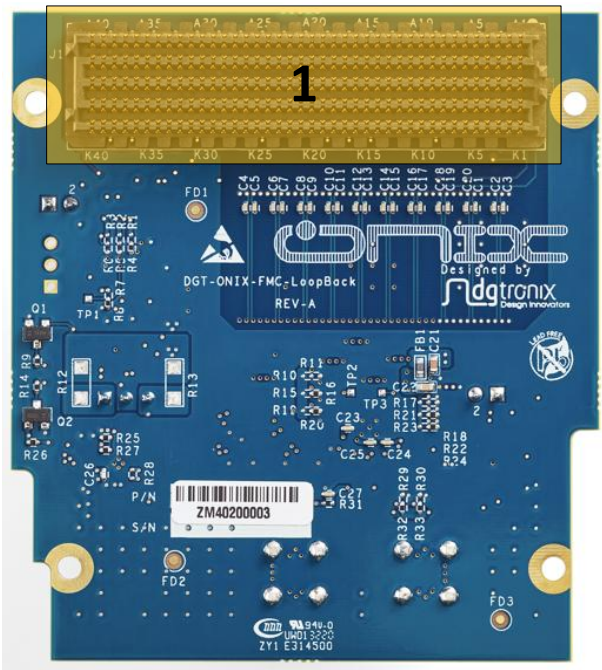


Figure 3: DGT-ONIX-FMC-LOOPBACK – Bottom Side Components

ID	RefDes	Component Description

1	J1	VITA 57.1 FMC HPC Connector
2	U5	Si570 serial I2C bus programmable XO (100MHz Default)
3	J6	Positive input - differential reference CLK
4	J7	Negative input - differential reference CLK
5	U3	Si53301 2:6 low-jitter Fanout Clock Buffer
6	J4	Reference Clock Source Header
7	U4	On-Board DC/DC Converter for VIO_B
8	J5	VIO_B Source Header
9	U2	I2C Level Translator
10	U1	32Kbit I2C EEPROM
11	J2	JTAG Loop Header

Table 3: DGT-ONIX-FMC-LOOPBACK Component Descriptions

3.5. FMC HPC Connector Onboard Loopback

The board provides loopback connections as shown in the next sections:

3.5.1. FMC MGT LoopBack Table:

FMC Pin Name	FMC Pin Number	<Loop To> (100nF Capacitor)	FMC Pin Name	FMC Pin Number
DP0_C2M_P	C2	<>	DP0_M2C_P	C6
DP0_C2M_N	C3	<>	DP0_M2C_N	C7
DP1_C2M_P	A22	<>	DP1_M2C_P	A2
DP1_C2M_N	A23	<>	DP1_M2C_N	A3
DP2_C2M_P	A26	<>	DP2_M2C_P	A6
DP2_C2M_N	A27	<>	DP2_M2C_N	A7
DP3_C2M_P	A30	<>	DP3_M2C_P	A10
DP3_C2M_N	A31	<>	DP3_M2C_N	A11
DP4_C2M_P	A34	<>	DP4_M2C_P	A14
DP4_C2M_N	A35	<>	DP4_M2C_N	A15
DP5_C2M_P	A38	<>	DP5_M2C_P	A18
DP5_C2M_N	A39	<>	DP5_M2C_N	A19
DP6_C2M_P	B36	<>	DP6_M2C_P	B16
DP6_C2M_N	B37	<>	DP6_M2C_N	B17
DP7_C2M_P	B32	<>	DP7_M2C_P	B12
DP7_C2M_N	B33	<>	DP7_M2C_N	B13
DP8_C2M_P	B28	<>	DP8_M2C_P	B8
DP8_C2M_N	B29	<>	DP8_M2C_N	B9
DP9_C2M_P	B24	<>	DP9_M2C_P	B4
DP9_C2M_N	B25	<>	DP9_M2C_N	B5

3.5.2. FMC LA Bank LoopBack:

FMC Pin Name	FMC Pin Number	<Loop To>	FMC Pin Name	FMC Pin Number
LA00_P_CC	G6	<>	LA01_P_CC	D8
LA00_N_CC	G7	<>	LA01_N_CC	D9
LA02_P	H7	<>	LA03_P	G9
LA02_N	H8	<>	LA03_N	G10
LA04_P	H10	<>	LA05_P	D11
LA04_N	H11	<>	LA05_N	D12
LA06_P	C10	<>	LA07_P	H13
LA06_N	C11	<>	LA07_N	H14
LA08_P	G12	<>	LA09_P	D14
LA08_N	G13	<>	LA09_N	D15
LA10_P	C14	<>	LA11_P	H16
LA10_N	C15	<>	LA11_N	H17
LA12_P	G15	<>	LA13_P	D17
LA12_N	G16	<>	LA13_N	D18
LA14_P	C18	<>	LA15_P	H19
LA14_N	C19	<>	LA15_N	H20
LA16_P	G18	<>	LA17_P_CC	D20
LA16_N	G19	<>	LA17_N_CC	D21
LA18_P_CC	C22	<>	LA19_P	H22
LA18_N_CC	C23	<>	LA19_N	H23
LA20_P	G21	<>	LA21_P	H25
LA20_N	G22	<>	LA21_N	H26
LA22_P	G24	<>	LA23_P	D23
LA22_N	G25	<>	LA23_N	D24
LA24_P	H28	<>	LA25_P	G27
LA24_N	H29	<>	LA25_N	G28
LA26_P	D26	<>	LA27_P	C26
LA26_N	D27	<>	LA27_N	C27
LA28_P	H31	<>	LA29_P	G30
LA28_N	H32	<>	LA29_N	G31
LA30_P	H34	<>	LA31_P	G33
LA30_N	H35	<>	LA31_N	G34
LA32_P	H37	<>	LA33_P	G36
LA32_N	H38	<>	LA33_N	G37

3.5.1. FMC HA Bank LoopBack:

FMC Pin Name	FMC Pin Number	<Loop To>	FMC Pin Name	FMC Pin Number
HA00_N_CC	F5	<>	HA01_N_CC	E3
HA00_P_CC	F4	<>	HA01_P_CC	E2
HA02_N	K8	<>	HA03_N	J7
HA02_P	K7	<>	HA03_P	J6
HA04_N	F8	<>	HA05_N	E7
HA04_P	F7	<>	HA05_P	E6
HA06_N	K11	<>	HA07_N	J10
HA06_P	K10	<>	HA07_P	J9
HA08_N	F11	<>	HA09_N	E10
HA08_P	F10	<>	HA09_P	E9
HA10_N	K14	<>	HA11_N	J13
HA10_P	K13	<>	HA11_P	J12
HA12_N	F14	<>	HA13_N	E13
HA12_P	F13	<>	HA13_P	E12
HA14_N	J16	<>	HA15_N	F17
HA14_P	J15	<>	HA15_P	F16
HA16_N	E16	<>	HA17_N_CC	K17
HA16_P	E15	<>	HA17_P_CC	K16
HA18_N	J19	<>	HA19_N	F20
HA18_P	J18	<>	HA19_P	F19
HA20_N	E19	<>	HA21_N	K20
HA20_P	E18	<>	HA21_P	K19
HA22_N	J22	<>	HA23_N	K23
HA22_P	J21	<>	HA23_P	K22

3.5.1. FMC HB Bank LoopBack:

FMC Pin Name	FMC Pin Number	<Loop To>	FMC Pin Name	FMC Pin Number
HB00_N_CC	K26	<>	HB01_N	J25
HB00_P_CC	K25	<>	HB01_P	J24
HB02_N	F23	<>	HB03_N	E22
HB02_P	F22	<>	HB03_P	E21
HB04_N	F26	<>	HB05_N	E25
HB04_P	F25	<>	HB05_P	E24
HB06_N_CC	K29	<>	HB07_N	J28
HB06_P_CC	K28	<>	HB07_P	J27
HB08_N	F29	<>	HB09_N	E28
HB08_P	F28	<>	HB09_P	E27
HB10_N	K32	<>	HB11_N	J31
HB10_P	K31	<>	HB11_P	J30
HB12_N	F32	<>	HB13_N	E31
HB12_P	F31	<>	HB13_P	E30
HB14_N	K35	<>	HB15_N	J34
HB14_P	K34	<>	HB15_P	J33
HB16_N	F35	<>	HB17_N_CC	K38
HB16_P	F34	<>	HB17_P_CC	K37
HB18_N	J37	<>	HB19_N	E34
HB18_P	J36	<>	HB19_P	E33
HB20_N	F38	<>	HB21_N	E37
HB20_P	F37	<>	HB21_P	E36

3.6. FMC VIO_B Supply:

The VIO_B voltage can be configured the following states:

1. Disconnected (for unused bank B application).
2. Connect directly to FMC_VADJ.
3. Connect to the on-board DC/DC converter which supply the optional voltages: 1.2V/2.5V/3.3V (see section 3.6.1).

The selection of the source can be done using J5 3-pin header as shown on Figure 4:

Figure 4: J5 VIO_B Header

3.6.1. DC/DC Converter Output Voltage:

The output voltage of the DC/DC converter can be selected by R48, R53, R56 (0ohm, 0603) resistors, as shown on Table 4 and Figure 5:

Output Voltage	R48	R53	R56
1.8V (Default)	✗	✗	✓
2.5V	✓	✗	✗
3.3V	✗	✓	✗

Table 4: DC/DC Output Select Resistors

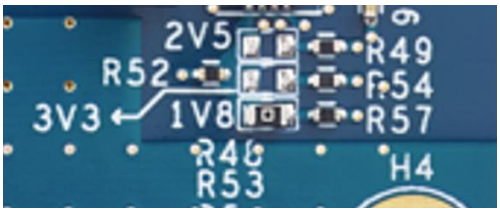


Figure 5: DC/DC Output Select Resistor

3.7. Clocks Distribution:

3.7.1. Clock Inputs:

The Si53301 (U3) can be referenced by both the on-board oscillator (U4) and the differential input via SMA connectors (J6, J7).

The reference clock can be selected by J4 header according to the following table:

Reference	J4 State
SMA	Connect
Oscillator	Disconnect

3.7.1.1. On-Board Oscillator (U4):

The Si570 serial I2C bus programmable XO provides a low-jitter clock with a user-programmable output frequency.

Parameter	Si570
Output Format	LVDS
Frequency Stability	$\pm 20PPM$
Frequency Range	$10 - 280MHz$
Default Frequency	100MHz
Supply Voltage	3.3V
I2C Address	0x55

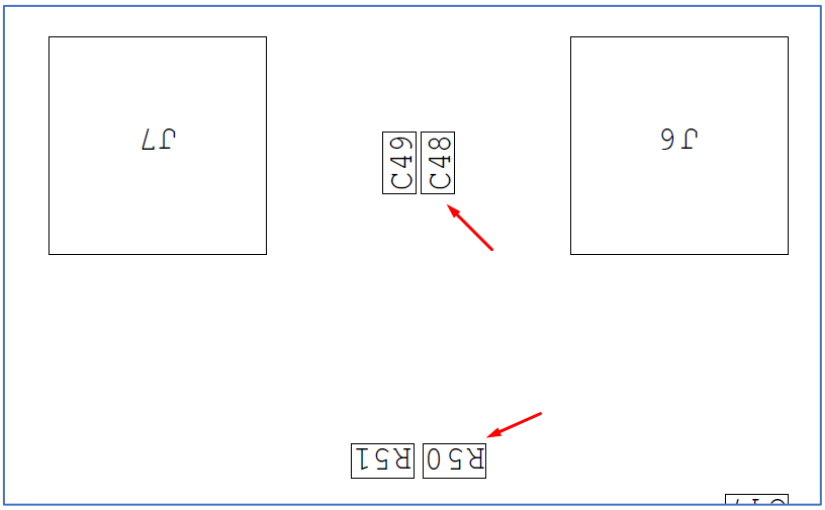
3.7.1.2. SMA Input:

J6 & J7 can be used for external clock source reference, J6 is the positive input, and J7 is the negative input.

By default, the input type is differential, however the input can be change to single-ended CMOS type by the following actions:

1. Replace C48 (100nF, 0402, 25V) with a 0ohm, 0402 resistor.
2. Remove R50 (49.9ohm, 0402).
3. Place 1Kohm, 0402 resistor in R31.

In this case, the input single-ended connector is J6 and J7 should be left unconnected.



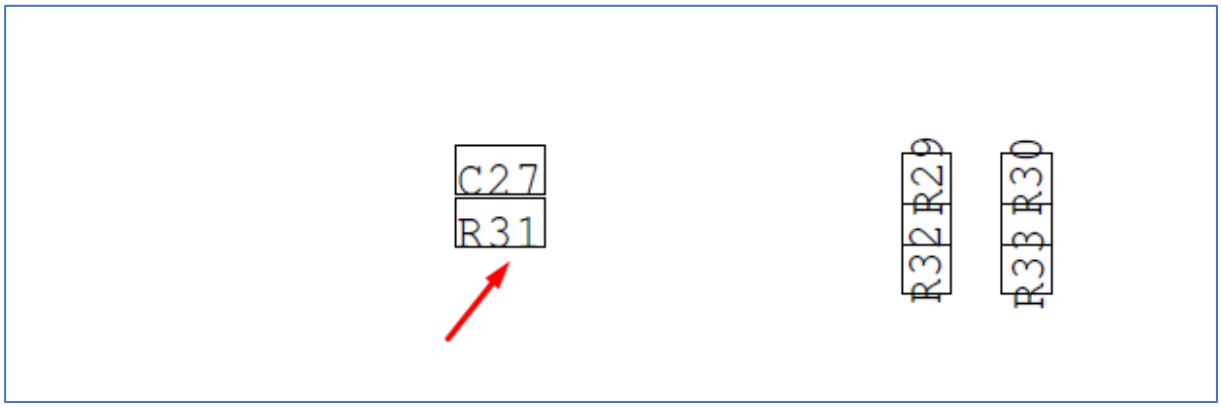


Figure 6 shows the components placement.

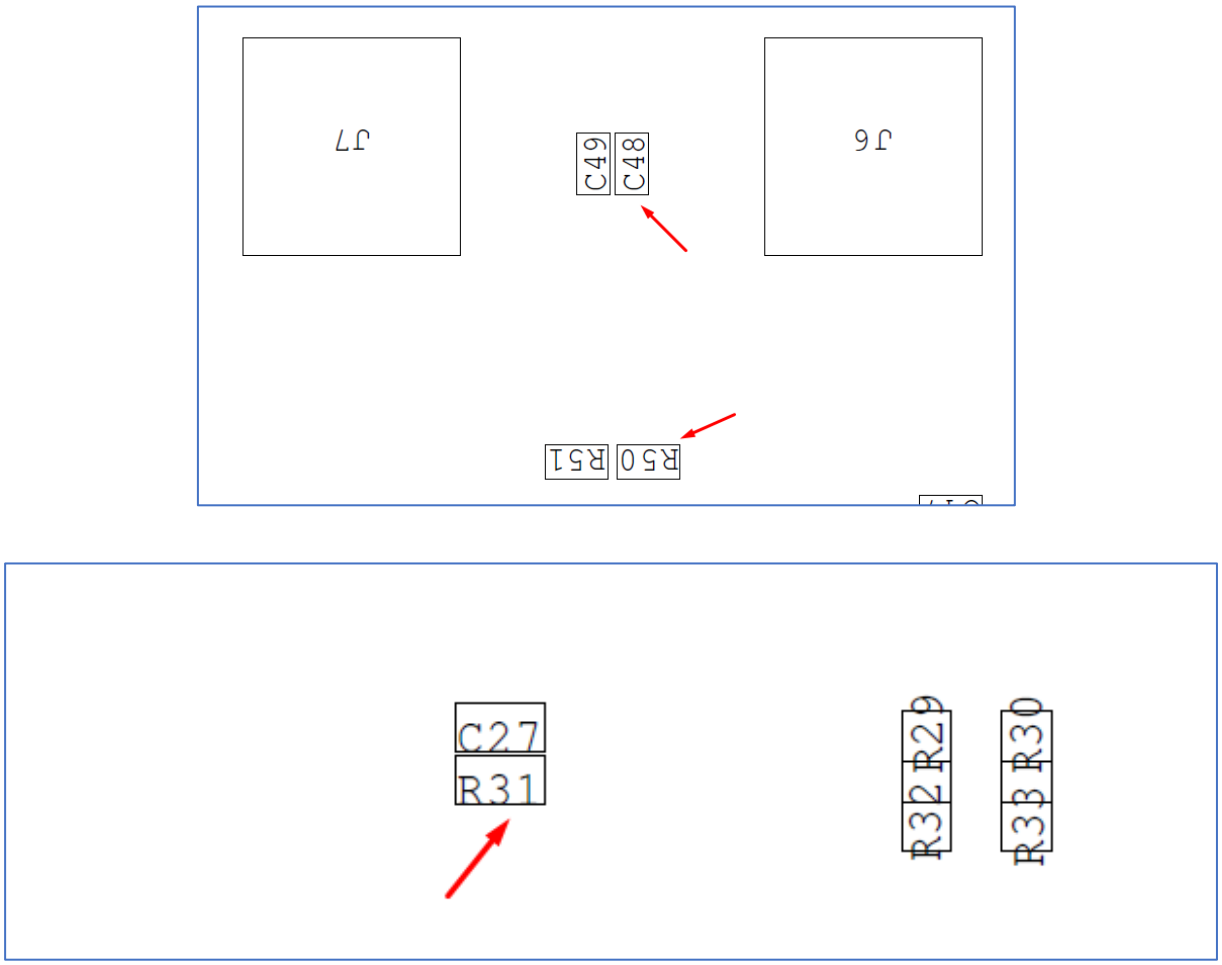


Figure 6: Single-Ended Replace Components

3.7.2. Clock outputs:

The board supply 6 differential clocks to the FMC HPC J1connector.

All of the 6 clocks are generated by the Si53301 fanout clock buffer.

Table 5 shows the U3 output connections to the J1 FMC HPC connector.

Net Name	U3 Pin Number	FMC PIN Number	Series Capacitor
GBT_CLK0_M2C_P	5	D4	100nF
GBT_CLK0_M2C_N	4	D5	100nF
GBT_CLK1_M2C_P	21	B20	100nF
GBT_CLK1_M2C_N	20	B21	100nF
FMC_CLK0_M2C_P	26	H4	None
FMC_CLK0_M2C_N	25	H5	None
FMC_CLK1_M2C_P	30	G2	None
FMC_CLK1_M2C_N	29	G3	None
FMC_CLK2_M2C_P	28	K4	None
FMC_CLK2_M2C_N	27	K5	None
FMC_CLK3_M2C_P	32	J2	None
FMC_CLK3_M2C_N	31	J3	None

Table 5: U3 Output Connection to J1 FMC HPC Connector

4. Board Specifications

4.1. Board Dimensions

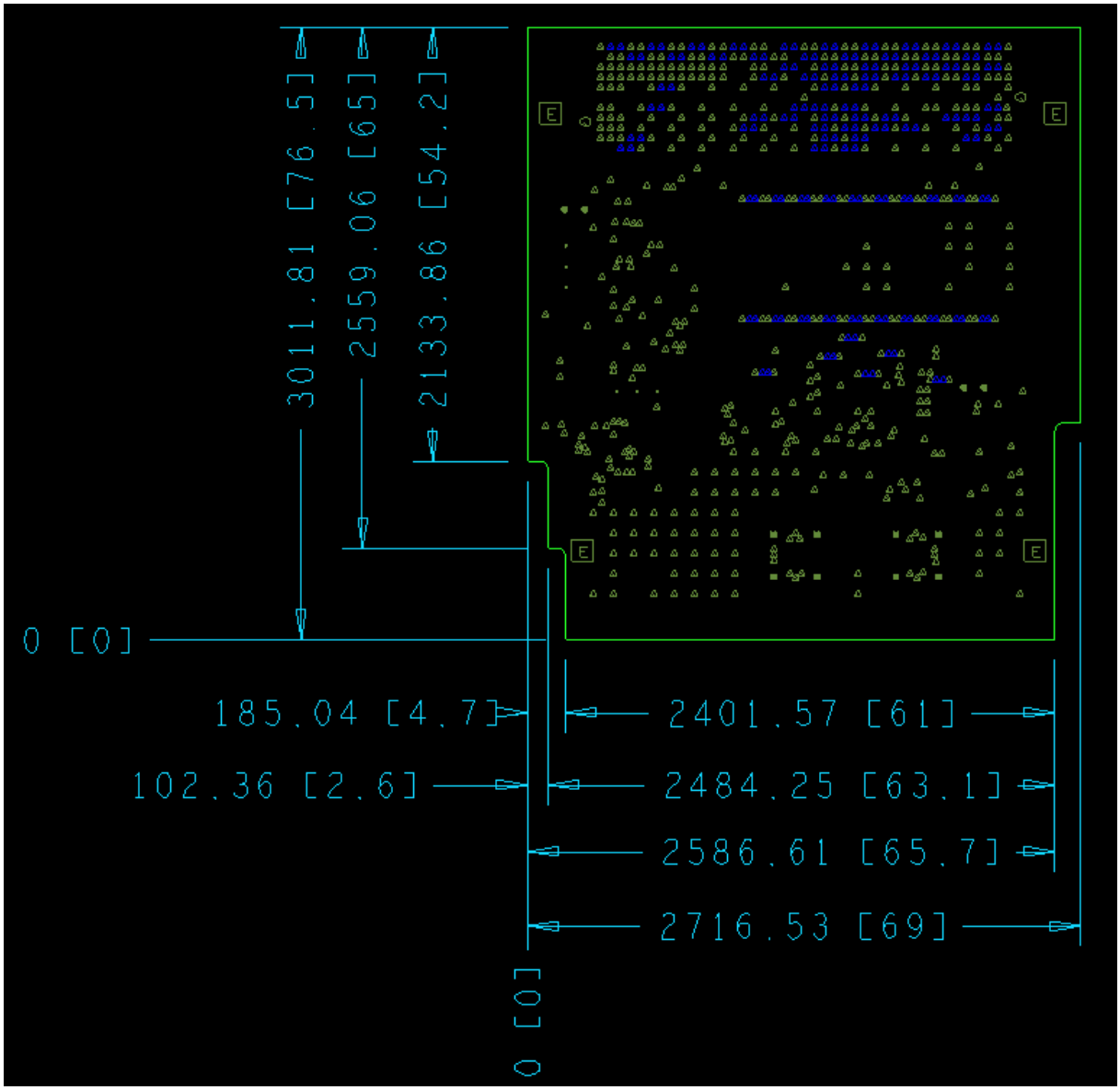


Figure 7 - Board Dimensions

Notes:

1. All dimensions are in mils [millimeters]
2. The dimensional diagram is for reference only

5. Order Information

5.1. Parts

Part Number	Description	Price
ONIX-FMC-LOOPBACK	FMC (VITA57.1) Loopback Mezzanine Board	Contact your local distributor

5.2. Related Products

Part Number	Description	Price
AVT-ONIX-VU440-1	ONIX Module XCVU440 -1 Device	Contact your local distributor
AVT-ONIX-VU440-2	ONIX Module XCVU440 -2 Device	Contact your local distributor
AVT-ONIX-PCIE-IPASS-8X-G	PCI Express to IPASS 8x module	Contact your local distributor
AVT-ONIX-KIT-IPASS-8X-G	PCI Express over Cable	Contact your local distributor

***For more info** http://www.onix.systems*