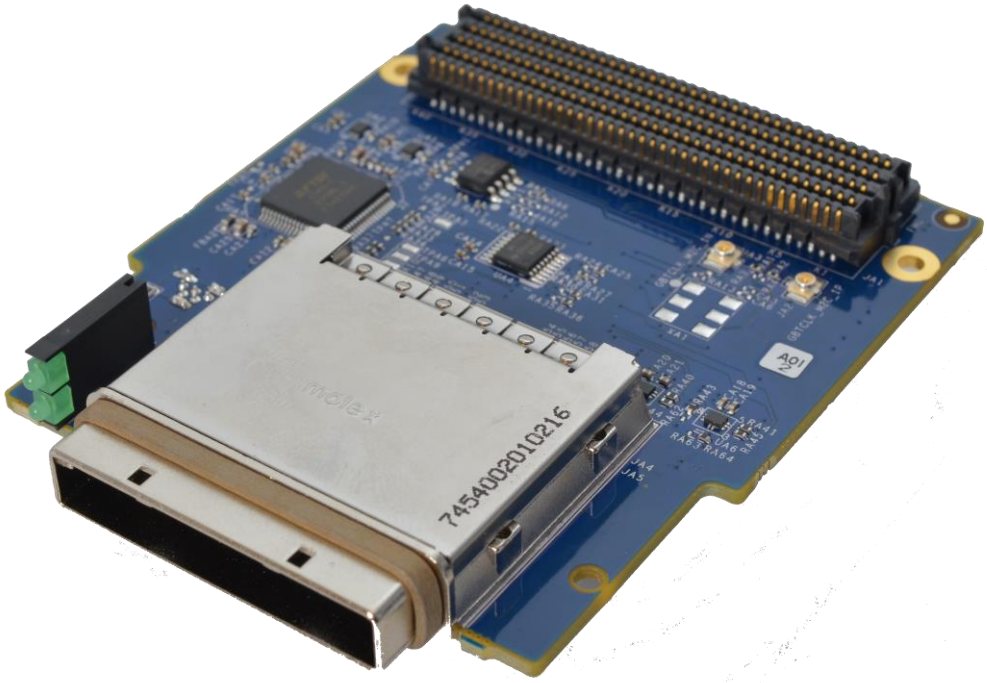
ASIC Prototyping Platforms



AVT-ONIX-FMC-IPASS-8X-G (A)
User Guide

Version 0.3

Table of Contents

Table of Figures

Tables

1. Revision History

The following table shows the revision history for this document.

Author / Company	Description	Revision	Date
ONIX D.T Ltd	Initial ONIX release	0.1	21/07/16
ONIX D.T Ltd	Updated Block Diagram design	0.2	01/09/16
ONIX D.T Ltd	Updated iPASS interface tables	0.3	25/01/17

Table 1 – Revision History

2. Reference Documents

Document	Source
FPGA Mezzanine Card (FMC) Standard	VITA
iPASS Interconnect Solutions	Molex

Table 2 – Reference Documents

3. AVT-ONIX-FMC-IPASS-8X Features

3.1. Overview

This document provides information regarding the AVT-ONIX-FMC-IPASS-8X module. The module is a VITA 57.1 compliant single width FMC HPC, designed for use with ONIX modules and more 57.1 compliant carrier cards.

The following chapters will describe the top-down information of FMC-IPASS Module.

3.2. Block Diagram

The AVT-ONIX-FMC-IPASS-8X board block diagram shown in Figure 1.

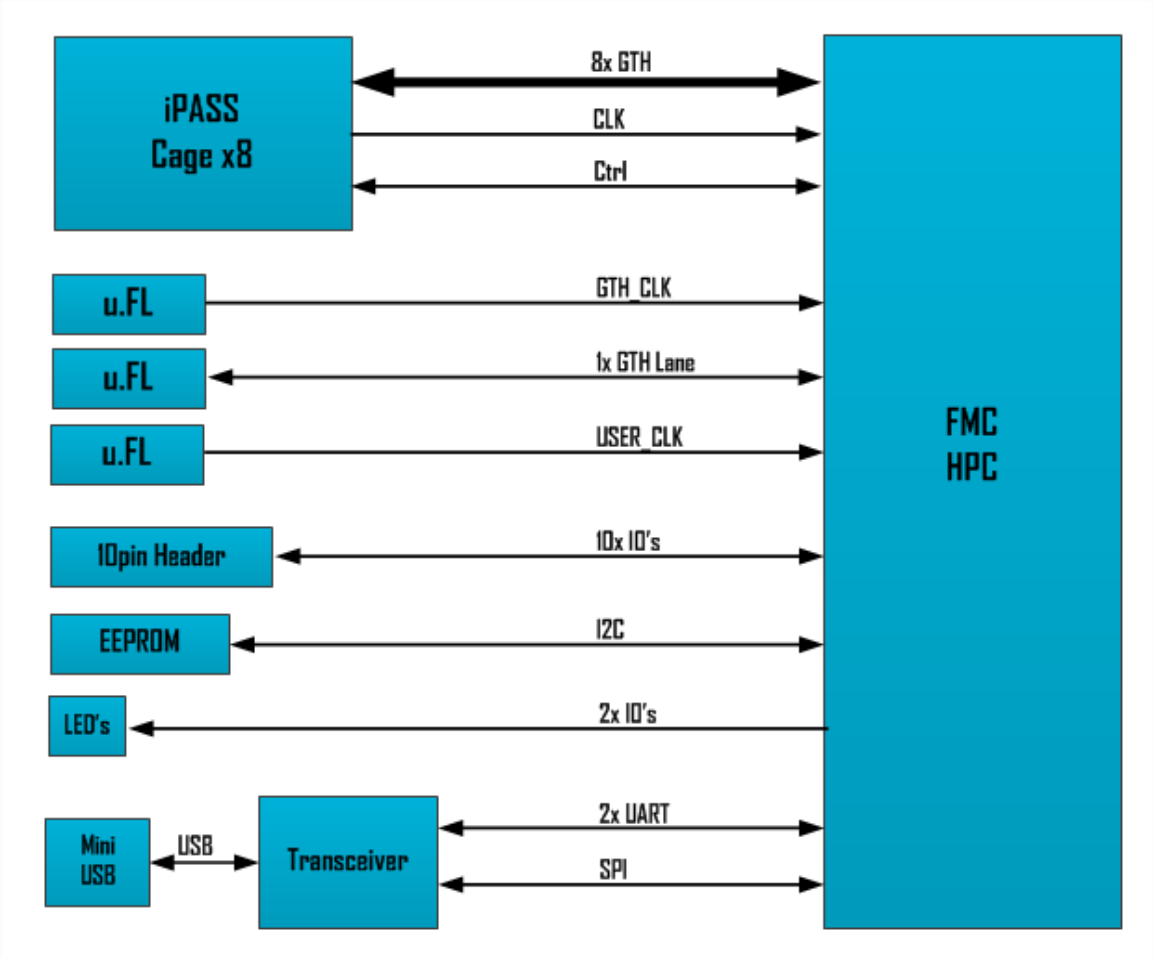


Figure 1 - AVT-ONIX-FMC-IPASS Block Diagram

3.3. Board Features

- VITA 57.1 FMC HPC connector
- 8x lanes up to 14Gbps for iPASS interface (fit to many signaling standards)
- 2x u.FL connector for GTH clock
- 4x u.FL connector for GTH lane (TX and RX)
- 2x u.FL connector for User clock
- 10pin Header for User
- Front Panel LED’s
- 2x UART interface (via Transceiver)
- 1x SPI interface (via Transceiver)
- On board clock oscillator for GTH ref clock (optional)

3.4. Feature Descriptions

The following figure shows the AVT-ONIX-FMC-IPASS-8X board. Each numbered feature that is referenced in Figure X is described in Table X.

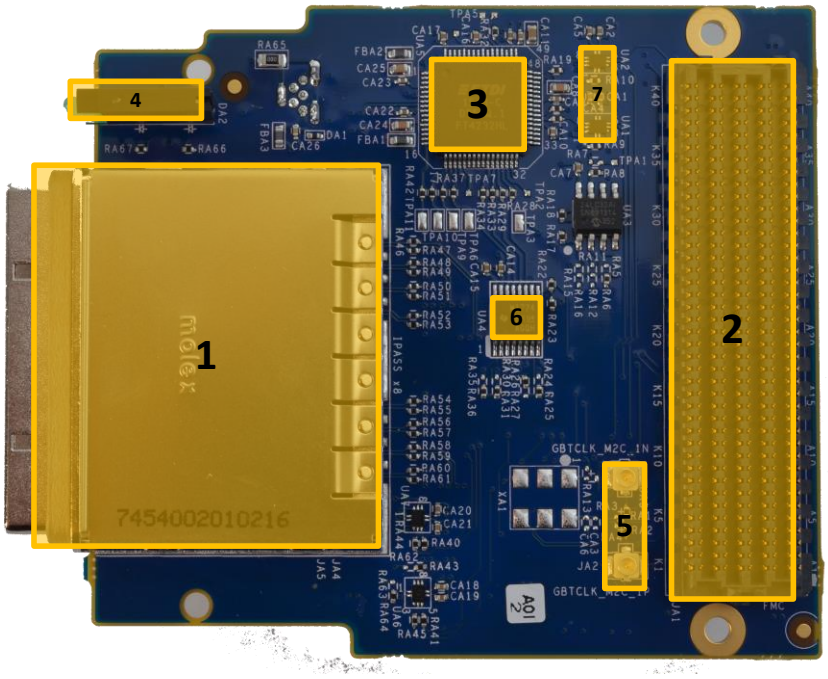


Figure 2 - AVT-ONIX-FMC-IPASS-8X – Top Board Components

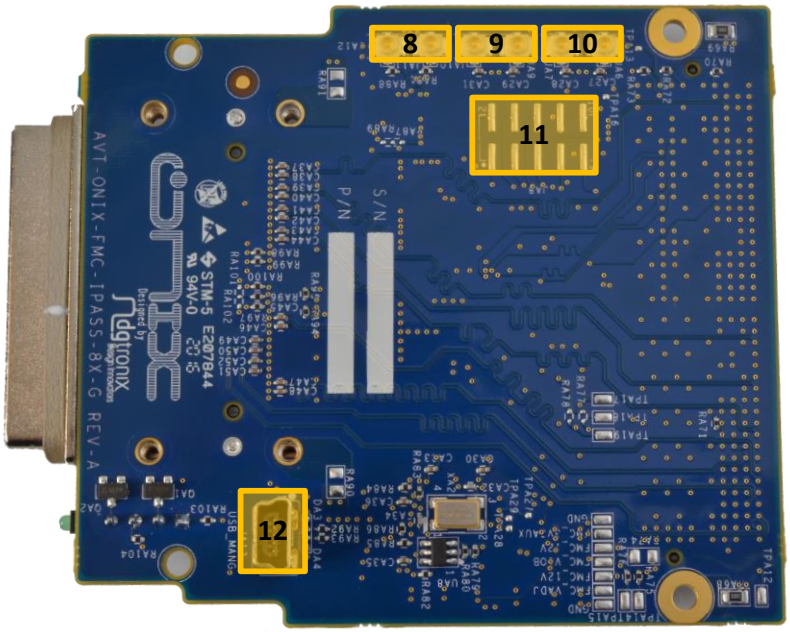


Figure 3 - AVT-ONIX-FMC-IPASS-8X – Bottom Board Components

ID	RefDes	Component Description
1	JA4	iPASS 8X Cage
2	JA1	FMC 400pin Connector
3	UA5	USB to UART/SPI Transceiver
4	DA2	Dual Front Panel LED's
5	JA2, JA3	GTH Input Reference Clock
6	UA4	Level Translator for SPI interface
7	UA1, UA2	Level Translator for UART interface
8	JA11, JA12	uFL connector for USER Clock
9	JA9, JA10	uFL connector for GTH TX Lane
10	JA6, JA7	uFL connector for GTH RX Lane
11	JA8	10x TP's/Header for USER IO's
12	JA13	Mini USB connector for UART/SPI interface

Table 3 - AVT-ONIX-FMC-IPASS-8X Component Descriptions

3.4.1. IPASS Interface

The 8x High Speed Lane performs data transfers at the rate of up to 14Gpbs (depending device type, Equalization ability, Cable type and length. The GTH reference clock is output from the iPASS connector. It should AC coupled on the carrier board.

3.4.1.1. Clock Signals

The following is the connection pin-out of Clock signals.

FMC Pin	Signal Name	iPASS Pin	iPASS Pin Name	Note
D4	IPASS_CLK_P	A14	CREFCLK+	CLK to FPGA
D5	IPASS_CLK_N	A15	CREFCLK-	

Table 4 - Clock Signal Pin-out

3.4.1.2. Control Signals

The following is the connection pin-out of Control signals.

FMC Pin	Signal Name	iPASS Pin	iPASS Pin Name	Note
H14	IPASS_SB_RTN	A19	SB_RTN	Input to FPGA
C10	IPASS_CPWRON	A21	CPWRON	Input to FPGA
H13	IPASS_CWAKE#	B20	CWAKE#	Output from FPGA
C11	IPASS_CPERST#	B21	CPERST#	Input to FPGA

Table 5 - Control Signals - Pin-out

3.4.1.3. High Speed Signals

The following is the connection list between the FMC and iPASS Connector.

FMC Pin	Signal Name	iPASS Pin	iPASS Pin Name	Note
C6	IPASS_RX_P0	B2	PERp0	RX to FPGA
C7	IPASS_RX_N0	B3	PERn0	
A2	IPASS_RX_P1	B5	PERp1	RX to FPGA
A3	IPASS_RX_N1	B6	PERn1	
A6	IPASS_RX_P2	B8	PERp2	RX to FPGA
A7	IPASS_RX_N2	B9	PERn2	
A10	IPASS_RX_P3	B11	PERp3	RX to FPGA
A11	IPASS_RX_N3	B12	PERn3	
A14	IPASS_RX_P4	B23	PERp4	RX to FPGA
A15	IPASS_RX_N4	B24	PERn4	
A18	IPASS_RX_P5	B26	PERp5	RX to FPGA
A19	IPASS_RX_N5	B27	PERn5	
B16	IPASS_RX_P6	B29	PERp6	RX to FPGA
B17	IPASS_RX_N6	B30	PERn6	
B12	IPASS_RX_P7	B32	PERp7	RX to FPGA
B13	IPASS_RX_N7	B33	PERn7	
C2	IPASS_TX_P0	A2	PETp0	TX from FPGA
C3	IPASS_TX_N0	A3	PETn0	
A22	IPASS_TX_P1	A5	PETp1	TX from FPGA
A23	IPASS_TX_N1	A6	PETn1	
A26	IPASS_TX_P2	A8	PETp2	TX from FPGA
A27	IPASS_TX_N2	A9	PETn2	
A30	IPASS_TX_P3	A11	PETp3	TX from FPGA
A31	IPASS_TX_N3	A12	PETn3	
A34	IPASS_TX_P4	A23	PETp4	TX from FPGA
A35	IPASS_TX_N4	A24	PETn4	
A38	IPASS_TX_P5	A26	PETp5	TX from FPGA
A39	IPASS_TX_N5	A27	PETn5	
B36	IPASS_TX_P6	A29	PETp6	TX from FPGA
B37	IPASS_TX_N6	A30	PETn6	
B32	IPASS_TX_P7	A32	PETp7	TX from FPGA
B33	IPASS_TX_N7	A33	PETn7	

Table 6 - High Speed Lanes Pin-out

3.4.2. USB to UART Bridge

The AVT-ONIX-FMC-IPASS board contains a FTDI FT4232HL USB to UART bridge device (UA5) which allows a connection between host computer and FPGA with a USB port. The USB cable (standard-A plug to host computer and mini-B plug to JA13 connector) is supplied in the Kit.

The following figure describes the connectivity of UART interface.

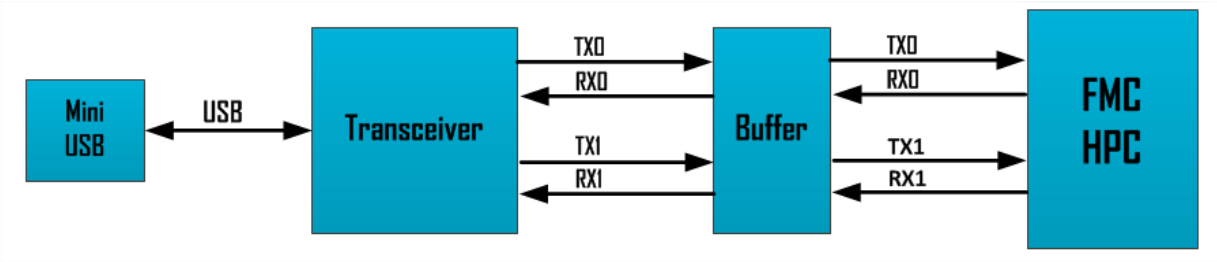


Figure 4 - USB to UART Bridge connectivity

The following is the connection between FPGA and UART.

FMC Pin	Signal Name	Direction	I/O Standard	Note
D11	UART0_TXD	Output	LVCMOS	To FPGA
H10	UART0_RXD	Input	LVCMOS	From FPGA
D12	UART1_TXD	Output	LVCMOS	To FPGA
H11	UART1_RXD	Input	LVCMOS	From FPGA

FTDI Device UA5		
Pin	**Function**	**Direction**
39	RX	Input
38	TX	Output
52	RX	Input
48	TX	Output

Table 7 - USB to UART Pin-out

3.4.3. USB to SPI Bridge

The AVT-ONIX-FMC-IPASS board contains a FTDI FT4232HL USB to SPI bridge device (UA5) which allows a connection between host computer and FPGA with a USB port. The USB cable (standard-A plug to host computer and mini-B plug to JA13 connector) is supplied in the Kit.

The following figure describes the connectivity of SPI interface.

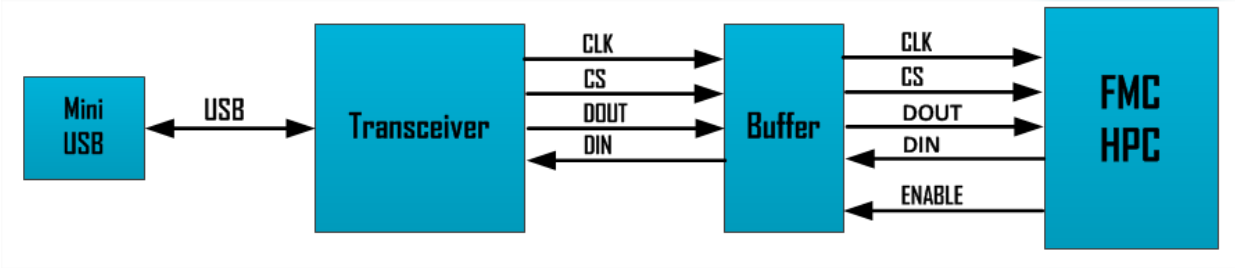


Figure 5 - USB to SPI Bridge connectivity

The following is the connection between FPGA and SPI.

FMC Pin	Direction	IO Standard	Net Name	Note
G6	Output	LVCMOS	SPIB_CLK_VADJ	SPI Clock - input to FPGA
H7	Output	LVCMOS	SPIB_DO_VADJ	SPI Dout - inout to FPGA
G9	Output	LVCMOS	SPIB_CS_VADJ	SPI Chip Select - input to FPGA
H8	Input	LVCMOS	SPIB_DI_VADJ	SPI Din - Output from FPGA
G10	Input	LVCMOS	SPIB_OEN	Enable = 1 \ Disable = 0 for SPI Buffer, Default = 0

FTDI Device UA5		
Pin	**Function**	**Direction**
26	CLK	Output
27	DO	Output
28	DI	Input
29	CS	Output

Table 8 - USB to SPI Pin-out

3.4.4. Panel LED's

The AVT-ONIX-FMC-IPASS board contains two panel LED's. The function of each LED's describes on the below table.

FMC Pin	Function	IO Standard	Color	Controlled by
D9	Panel LED Top	LVCMOS	Green	FPGA
G7	Panel LED Bottom	LVCMOS	Green	FPGA

Table 9 - Panel LED's

3.4.5. U.FL Connectors

The board contains eight uFL connectors for the following:

1. GTH Lane TX and RX
2. GTH input reference clock
3. USER input clock

FMC Pin	IO Standard	RefDes	Signal Name
D20	LVDS	JA11	UFL_CLK_LA.17_P_CC
D21		JA12	UFL_CLK_LA.17_N_CC
B20	LVDS	JA2	UFL_GBTCLK_M2C_1P
B21		JA3	UFL_GBTCLK_M2C_1N
B28	-	JA10	GTH_TX_09_P
B29		JA9	GTH_TX_09_N
B8	-	JA6	GTH_RX_09_P
B9		JA7	GTH_RX_09_N

Table 10 - User uFL connectors Pin-out

3.4.6. GPIO's Header

The following is the connection between the USER Header and FMC connector.

FMC Pin	RefDes	Signal Name
H16	JA8.1	GPIO_VADJ_1
H17	JA8.2	GPIO_VADJ_2
G15	JA8.3	GPIO_VADJ_3
G16	JA8.4	GPIO_VADJ_4
D17	JA8.5	GPIO_VADJ_5
D18	JA8.6	GPIO_VADJ_6
C18	JA8.7	GPIO_VADJ_7
C19	JA8.8	GPIO_VADJ_8
H19	JA8.9	GPIO_VADJ_9
H20	JA8.10	GPIO_VADJ_10

Figure 6 - GPIO Header pin-out

4. Board Specifications

4.1. Board Dimensions

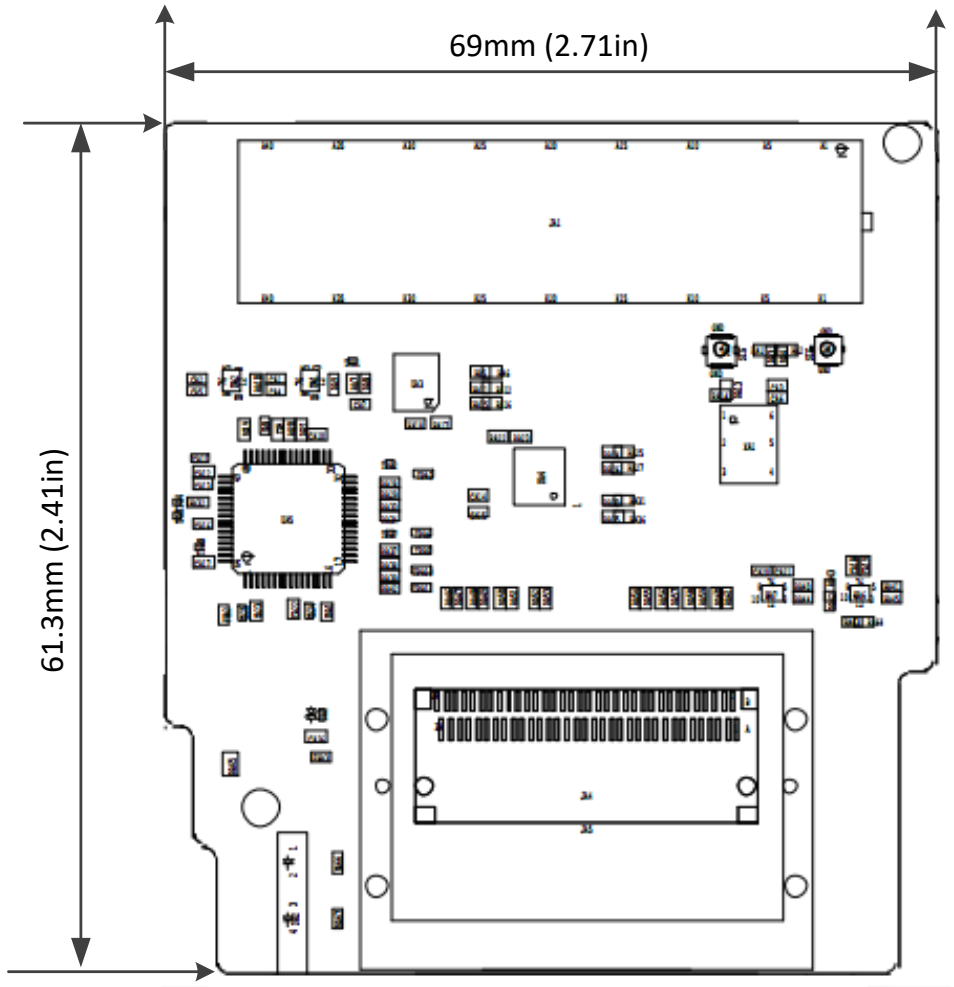


Figure 7 - Module Dimensions

Notes:

1. All dimensions are in millimeters
2. The dimensional diagram is for reference only

5. Order Information

5.1. Parts

Part Number	Description	Price
AVT-ONIX-FMC-IPASS-8X-G	FMC to IPASS 8x Lanes	Contact your local distributor

5.2. Related Products

Part Number	Description	Price
AVT-ONIX-VU440-1	ONIX Module XCVU440 -1 Device	Contact your local distributor
AVT-ONIX-VU440-2	ONIX Module XCVU440 -2 Device	Contact your local distributor
AVT-ONIX-PCIE-IPASS-8X-G	PCI Express to IPASS 8x module	Contact your local distributor
AVT-ONIX-KIT-IPASS-8X-G	PCI Express over Cable	Contact your local distributor

For more info http://www.onix.systems

6. Appendix

6.1. Mating Cable

The AVT-ONIX-FMC-IPASS-8X contain iPASS connector. iPASS is Interconnect Solutions provide host board and backplane connectors, as well as cable assemblies for SAS, PCIe, Ethernet, InfiniBand and Fiber Channel internal and external systems.

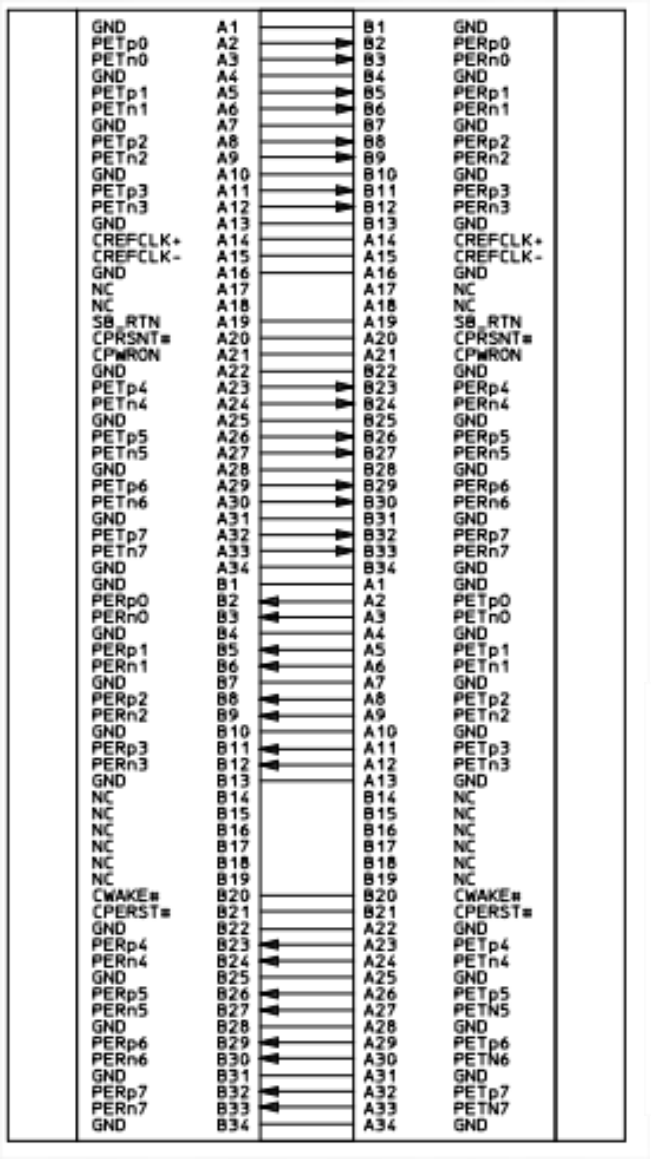
iPass connector Offering a full interconnect system that enables flexible speed compatibility for applications up to 14 Gbps (depending cable length ,device type and PCB layout quality).

The below is a part list of possible mating cables for the iPASS receptacle.

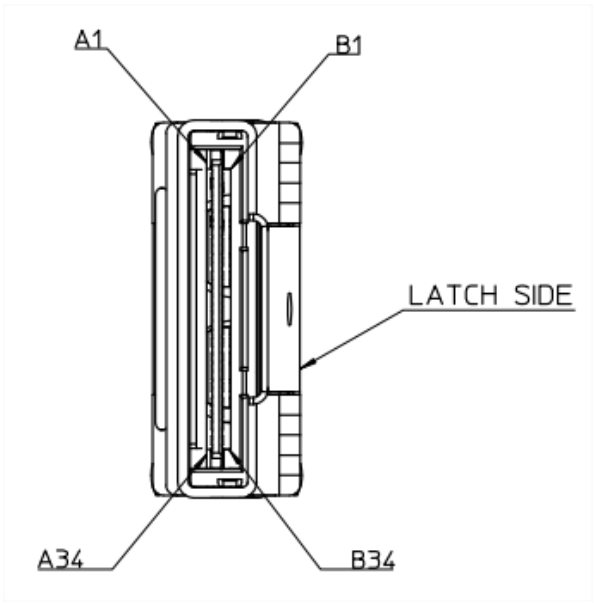
P/N	LENGTH	GAGE	TOLERANCE	JACKET RATING
74546-0801	1M	28	0.05M	VW1
74546-0802	2M	28	0.05M	VW1
74546-0803	3M	28	0.05M	VW1
74546-0804	4M	28	0.10M	VW1
74546-0805	5M	26	0.10M	CL2
74546-0806	6M	26	0.13M	CL2
74546-0807	7M	24	0.13M	CL2
74546-0808	8M △	24	0.13M	CL2
74546-0809	9M △	24	0.15M	CL2
74546-0810	10M △	24	0.15M	CL2
74546-0813	0.5M	28	0.03M	VW1

Table 11 - Mating Cables for iPass connector

6.2. Pin-out Cable



GND	A1		B1	GND	
PETp0	A2		B2	PERp0	
PETn0	A3		B3	PERn0	
GND	A4		B4	GND	
PETp1	A5		B5	PERp1	
PETn1	A6		B6	PERn1	
GND	A7		B7	GND	
PETp2	A8		B8	PERp2	
PETn2	A9		B9	PERn2	
GND	A10		B10	GND	
PETp3	A11		B11	PERp3	
PETn3	A12		B12	PERn3	
GND	A13		B13	GND	
CREFCLK+	A14		A14	CREFCLK+	
CREFCLK-	A15		A15	CREFCLK-	
GND	A16		A16	GND	
NC	A17		A17	NC	
NC	A18		A18	NC	
SB_RTN	A19		A19	SB_RTN	
CPRSNT#	A20		A20	CPRSNT#	
CPWRON	A21		A21	CPWRON	
GND	A22		B22	GND	
PETp4	A23		B23	PERp4	
PETn4	A24		B24	PERn4	
GND	A25		B25	GND	
PETp5	A26		B26	PERp5	
PETn5	A27		B27	PERn5	
GND	A28		B28	GND	
PETp6	A29		B29	PERp6	
PETn6	A30		B30	PERn6	
GND	A31		B31	GND	
PETp7	A32		B32	PERp7	
PETn7	A33		B33	PERn7	
GND	A34		B34	GND	
GND	B1		A1	GND	
PERp0	B2		A2	PETp0	
PERn0	B3		A3	PETn0	
GND	B4		A4	GND	
PERp1	B5		A5	PETp1	
PERn1	B6		A6	PETn1	
GND	B7		A7	GND	
PERp2	B8		A8	PETp2	
PERn2	B9		A9	PETn2	
GND	B10		A10	GND	
PERp3	B11		A11	PETp3	
PERn3	B12		A12	PETn3	
GND	B13		A13	GND	
NC	B14		B14	NC	
NC	B15		B15	NC	
NC	B16		B16	NC	
NC	B17		B17	NC	
NC	B18		B18	NC	
NC	B19		B19	NC	
CWAKE#	B20		B20	CWAKE#	
CPERST#	B21		B21	CPERST#	
GND	B22		A22	GND	
PERp4	B23		A23	PETp4	
PERn4	B24		A24	PETn4	
GND	B25		A25	GND	
PERp5	B26		A26	PETp5	
PERn5	B27		A27	PETN5	
GND	B28		A28	GND	
PERp6	B29		A29	PETp6	
PERn6	B30		A30	PETN6	
GND	B31		A31	GND	
PERp7	B32		A32	PETp7	
PERn7	B33		A33	PETN7	
GND	B34		A34	GND	



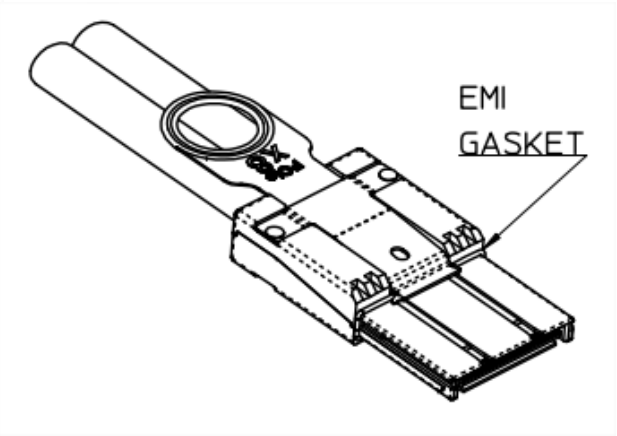


Table 12 - Molex pin-out cable